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Original Article

Design of an Active-Loaded Differential Voltage-Controlled Oscillator (VCO) Using Double-Gate MOSFET

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Abstract *- A differential cross-coupled Voltage Controlled Oscillator (VCO) has been designed using the Double-Gate (DG) MOSFET for VHF applications. The DG MOSFET exhibits superior noise immunity with its high noise figure and is suitable for low-power, high-frequency applications. The proposed VCO has been designed using a differential topology with improved power consumption, design flexibility, and noise reduction. This also improves the high-frequency performance of existing differential amplifiers. Thereafter, the proposed VCO was compared with fabrication and design methods, particularly Silicon-based CMOS and Single-Gate (SG) MOSFET VCOs, as possible alternatives. Various printed circuit board (PCB) design practices were followed to minimise the noise and improve the overall efficiency of the circuitry. Key parameters for the analysis of this VCO are the output power, phase noise, and figure of merit, which have been realised as -2.91 dBm at peak and -69.79 dBc/Hz at 1 MHz, respectively. The power consumption of the designed VCO is 36 mW.*

Keywords *- MOSFET, Double-Gate MOSFET, Differential amplifier, Microelectronics, Nanotechnology, VLSI, VCO.*

1. Introduction

A Voltage Controlled Oscillator (VCO) is a frequency oscillator whose output frequency depends on the voltage at a particular node in circuitry. This node is usually one that is connected to a variable capacitor known as a varactor diode or variable inductor. As the reverse bias voltage across the varactor diode changes, its capacitance varies. The capacitance forms a part of the Resistor-Capacitor (RC) or Inductor-Capacitor (LC) tank circuit, effectively providing a variable frequency output [1]. Currently, there are three common forms of VCOs, which include the Hartley oscillator (which uses inductive coupling), the Colpitts oscillator (which uses capacitive coupling) and the less-popular Clapp oscillator (similar to the Colpitts oscillator but changes the capacitive coupling of the base or gate of the transistor to prevent cross-coupling from the emitter or source) [1, 2].

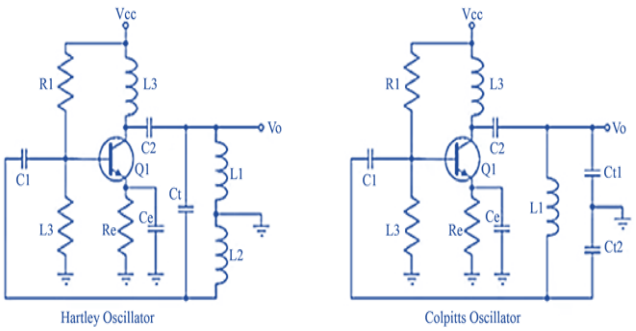

Fig. 1 VCO architectures showing differences in output coupling

An oscillator uses a resonator (an LC or RC tank circuit), which overcomes its losses electrically by achieving stability depending on the characteristics and nonlinearities of the entire oscillator. For a single-transistor VCO, a start-up transconductance $g_{m(START)}$ must be achieved, which will change to a new transconductance $g_{m(CURRENT)}$. There is a given transconductance gm for a given resonant frequency.

$g_{m(RESONATE)}$. For sustained, stable oscillation to occur:

$$g_{m(CURRENT)} + g_{m(RESONATE)} = 1 \quad (1)$$

The stability of an oscillator can be affected by many factors, which can be separated into three aspects:

- Start-up conditions not being met [3] – The LC-tank circuit must be provided with sufficient voltage to ensure sustained oscillations. The capacitor of the LC circuit typically requires this. Using a standard capacitor with a fixed capacitance can ensure this, given that it will charge accordingly and be able to maintain oscillation. If the oscillator is not biased correctly and cannot meet the initial start-up condition of the resonator circuitry, the output will not be present;
- Frequency effects – the output frequency of the VCO should not be affected by a shift in supply voltage, which is known as frequency pushing [4]. This can be avoided by utilising measures to control the supply voltage, preventing any fluctuation (an increase or decrease), and ensuring the control voltage of the

resonator circuit is broad. Frequency pushing can cause substantial degradation in phase noise, given that the circuit will also be easily affected by power-supply noise [5];

- Varactor-related effects – This component is essential to the operation of the VCO. There must be careful attention paid to the tuning gain (which should be reduced to reduce the phase noise of the oscillator) and tuning voltage (a reverse-biased varactor may become forward-biased, but the tuning voltage should never be zero, which will seize oscillation) [6]. Design methods to improve the varactor's behaviour in the resonator circuit include a back-to-back varactor configuration [7], maintaining a high voltage (> 50% of the supply voltage) around the varactor output node to ensure a reverse-bias voltage can be maintained [8].

The variations in design from the literature are noted, where VCOs, shown in Figure 1, may be designed and include optimisations. Son et al. [8] have designed a widely tunable K-band voltage-controlled oscillator, which, by definition, can be used in microwave frequencies, i.e. 18 GHz – 27 GHz. The objective of this Silicon-based CMOS design was to provide three banks of capacitors in conjunction with a varactor diode to increase the tuning range of the LC-tank circuit. The capacitor banks equate to approximately 352.5 fF to 526 fF, as the total equivalent capacitance is 462.6 fF to 709.1 fF, with the varactor capacitance being 110.1 fF to 183.1 fF. Considering the work of this paper, it is important to create a large tuning range to maximise the tuning voltage and prevent saturation of the resonator.

An active-loaded configuration was used in the previous study, which makes it closely related to the push-pull configuration in Silicon-based CMOS and Field-Effect Transistor (FET) biasing by visual inspection. Designed by Zhang [10], A VCO utilising the push-push dual band cross-coupled configuration exhibited an excellent phase noise of -108.57 dBc/Hz at 10 MHz. However, the design of this VCO was considered carefully, as the tail current source is known for readily introducing phase noise. Elevated levels of phase noise and the minimised tuning range are owed to the addition of the tail current source, which was helped by extra capacitors in the LC resonator and low-pass filters between the varactor and its voltage node, which is injected into the push-push transistor pair.

Considering the differential amplifier being used in VCO design, this has been investigated by Khatoon and Chandel [11], which exhibited substantial ability, consuming 3.1 mW, at the maximum tuning voltage of 2.3 V. This method of design also utilised operational amplifiers instead of FETs. This significantly affects the design process. A buffer circuit would be added at the output of a VCO to provide a higher output power. The buffer may be built using a general-purpose Operational Amplifier (Op-Amp) or transistors (BJTs or MOSFETs). A cascode amplifier was used by Trotta et al. [12], and a Darlington-based topology for the output stage was used by Han et al. [13]. From the analysis of the aforementioned literature, a list of parameters ought to be evaluated to characterise, compare and specify suitable applications for the proposed VCO. These parameters include output power, phase noise, tuning voltage characterisation, and tuning characteristics. The output power can be used to determine the peak-to-peak voltage of the output waveform/carrier Vpk-pk.

For the design of the VCO, a differential topology will be used [14]. This has been reviewed as a possible alternative to the Colpitts and Hartley oscillator. Kackar et al. [16] have highlighted the expansiveness of this oscillator model, showing the addition of multiple transistor stages which could be added to achieve different functional specifications. These specifications may include a wider bandwidth, which uses a 7-stage Differential Voltage Controlled Ring Oscillator (DRVCO), or a high-speed design which uses a 10-stage DRVCO. The transistor stages play their respective roles in driving other transistors to achieve larger output swings for a larger bandwidth or better latch times for faster response times.

The proposed VCO of this work uses a two-stage differential architecture, where two DG MOSFETs, acting as current sources, will be used to drive their successive signal-in DG MOSFETs in the signal chain, forming part of a current mirror constructed using two general-purpose N-Channel MOSFETs. This can be seen in Figure 3, given the differential amplifier designed on previous studies. The DG MOSFET has shown to be a low-power, high-frequency transistor, given its lower drain-source VDS to maintain an adequate drain current. An output buffer would not be used in this design, as stand-alone power and frequency characteristics must be observed, which could be manipulated by adding a buffer.

The differential oscillator was investigated as an nMOS van-der-Pol differential oscillator by Buccoleri et al. [17], which was developed to overcome the Groszkowski effect, which is the dependence of the oscillation frequency on the transistor current. This is undesirable, as this gives rise to jitter. Using the van-der-Pol differential oscillator, the frequency shift of the oscillation frequency from the resonant frequency is reduced.

Authors would have to deliberate using a variable inductor or variable capacitor to design the tank circuit. Mansour et al. [19] have incorporated a high-Q off-chip inductor into the 130nm CMOS process, yielding a 166% tuning range. However, the varactor diode has also been used in high-frequency applications but provides a lower tuning range, as shown by [21].

This work aims to achieve a sinusoidal output with a maximum RMS value (VRMS) of 177 mV and peak-to-peak voltage (Vpk-pk) of 500 mV. This signal is large enough to be used with a high-gain transmit (TX) amplifier for applications in Frequency Modulation (FM) or aircraft communications [22], which is the intended frequency band of operation. Since it will be an unmodulated signal, it can also function as a carrier frequency in FM. Given a Vpk-pk of 500 mV, the resulting transmit power will be approximately -2 dBm at peak. The load will be 50 Ω, which will be seen by the VCO as a standard BNC output port. It is also favourable to maintain a phase noise calculation of -50 dBm for the 70 – 100 MHz frequency range. This will be potentially achieved by reducing the effect of all noise sources (reduce thermal noise by keeping resistor values low, employing noise minimisation techniques in printed circuit board (PCB) design, utilise a hyper abrupt varactor diode for its small tuning range and reducing bias voltage [23]. The hyperabrupt diode is readily available and provides good linearity, i.e. re-verse-bias voltage vs capacitance.

The second harmonic is to be included by design. This will result in the inclusion of the frequency range of 140 – 200 MHz in the analysis of the proposed VCO. A working PCB design with schematic capture, while considering the above-mentioned specifications, i.e. reduction in noise, power consumption and signal integrity, is to be included.

The DG MOSFET, as shown in Figure 2 [21], is the subject of this research as a continuation of the analysis, where the active-loaded differential amplifier was designed using the DG MOSFET. The testing of this simulation reveals low power consumption for a similar output power compared to the cited works. The high-frequency behaviour is further investigated in the testing of the proposed VCO. The testing and evaluation of the proposed VCO will verify if the DG MOSFET is a suitable replacement for the SG MOSFET and current CMOS designs in high-frequency, low-power applications such as the VCO. This manuscript has been organised as follows: Section 2 outlines the design process of the designed VCO, i.e. current and voltage requirements, filtering, schematic capture and printed circuit board (PCB) design and routing. Section 3 outlines the testing of key parameters outlined by the literature study and compares the designed VCO to the aforementioned literature. Finally, Section 4 concludes the future work, which would be recommended for the designed VCO.

2. Design and Implementation of VCO using the DG MOSFET

Following the design of the active-loaded differential amplifier, the model shown in Figure 3 dictates the architecture of the VCO be designed in this literature, given that the differential topology and its active-loading principles were utilised in previous study.

2.1. Design of Resonator Circuit

Considering a resonator tank circuit for a frequency spectrum of 70 – 100 MHz, Equation 2 can be used to determine the resonant frequency for an LC resonator [24]:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

2.2. Current Biasing of DG MOSFETs

To utilise a large range of capacitance values of the varactor diode, a supply voltage of 9 V should be chosen. Given a maximum $V_{pk\text{-}pk}$ of *500 mV*, and V_{RMS} of *177 mV*, the equivalent maximum transmit power P_T is:

$$P_T(dBm) = 20\ \log_{10}\left(\frac{V_{RMS}}{\sqrt{\frac{Z}{1000}}}\right) \tag{3}$$

where Z is the impedance (Z = 50 Ω), thus by solving $P_T \approx$ -2 dBm. Converting P_T to watts,

$$P_T(watts) = \frac{10^{\frac{P_T(dBm)}{10}}}{1000}$$

Solving, P_T(watts) ≈ *0.63 mW*. Given this transmit power, and considering the V_{RMS} of the output waveform, the drain current I_D can be calculated as:

$$I_D = \frac{P_T(watts)}{V_{RMS}} \tag{4}$$

$$I_D \approx 4\ mA$$

The drain current of *2 mA* must be maintained through U1 and U3, and U2 and U4 to equate to *4 mA*. To bias the current mirror for a drain current of *4 mA*, R_{16} is the resistor at the drain of the current mirror formed by M1 and M2 in Figure 3 needs to be recalculated:

$$R_{16} = \frac{Positive\ supply - Negative\ supply}{desired\ drain\ current} \tag{5}$$

where the positive supply in this application is *9 V*, and the negative supply is 0 V. Thus, R_{16} is *2.2 kΩ*. It is required to choose a specified gate-2 to source voltage $V_{G2\text{-}S}$. For design simplicity, $V_{G2\text{-}S} \approx 4\ V$ conveniently depicts the I_D–V_{GS} characteristics in the datasheet of the BF998 DG MOSFET.

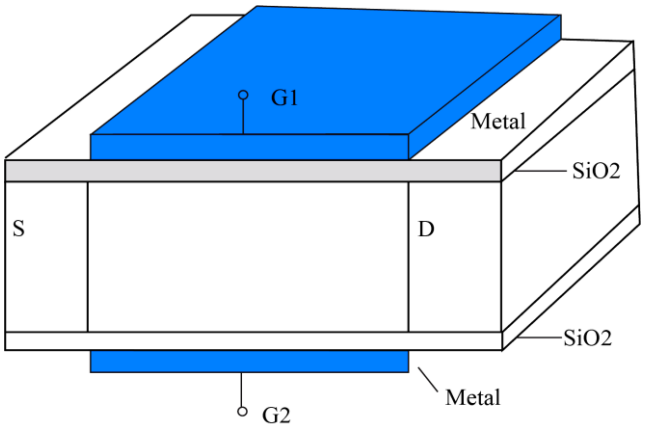

Fig. 2 Schematic of the Double-Gate MOSFET (S: Source, D: Drain, G1 and G2: gate-1 and gate-2, SiO2: Silicon dioxide).

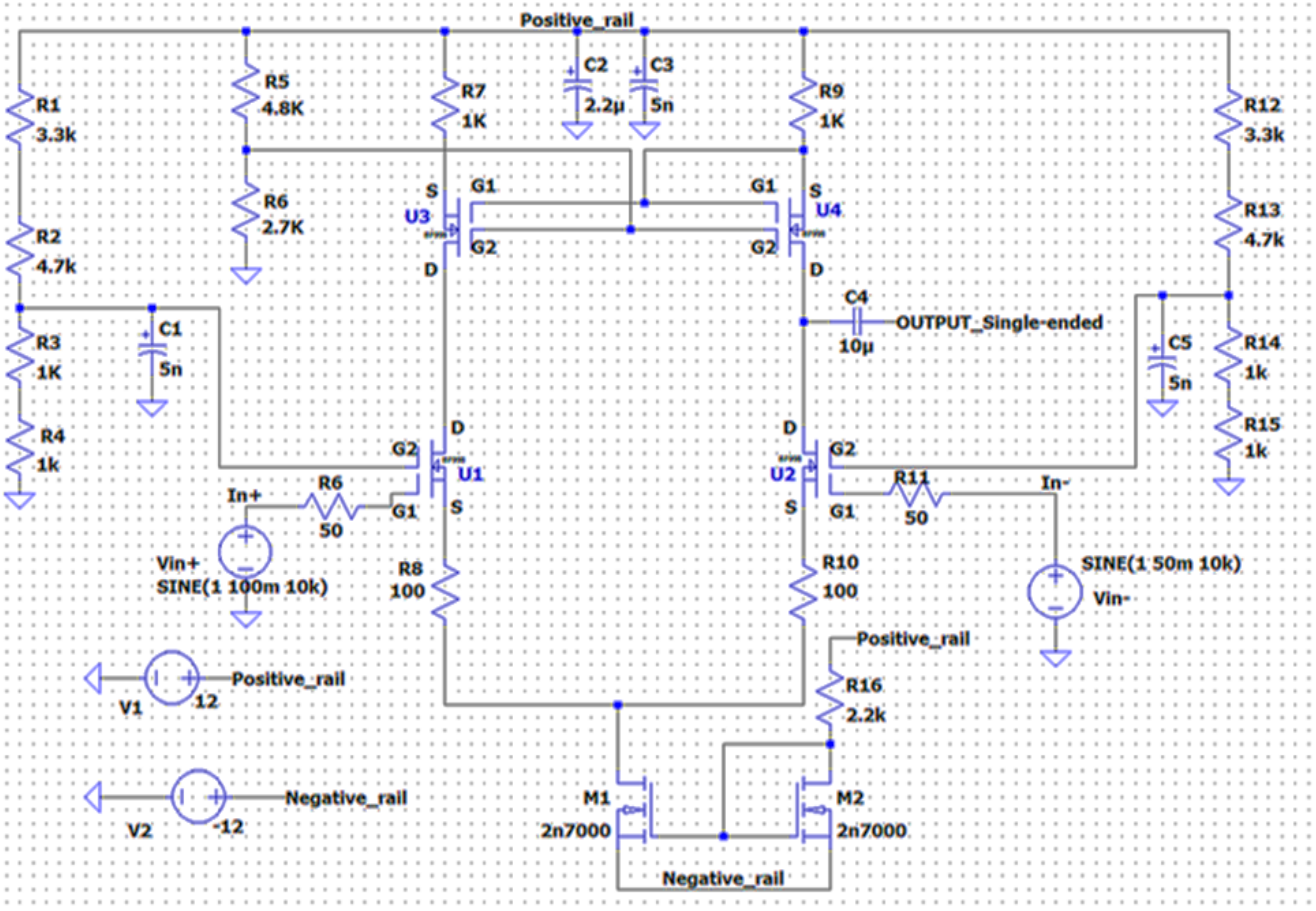

Fig. 3 Proposed active-loaded differential amplifier, which will be adapted for the proposed VCO

From Equation 1, the oscillating DG MOSFETs (U3 and U4, as seen in Figure 3) should maintain a similar transconductance g_m. This can be achieved by biasing both DG MOSFETs in an identical manner. The resulting resonant circuits, including U3 and U4, are shown in Figure 4. Figure 4 includes additions to the resonator circuit, such as R_2 and R_3, which introduce a DC bias. R_1 and R_4 provide the required source voltage V_S.

According to the datasheet [25], to maintain a drain current of *2 mA*, with a $V_{G2\text{-}S}$ of *4 V*, $V_{G1\text{-}S}$ must be *-0.4 V*. The dc bias of V_{G1} for U3 and U4 are determined by R_2 and R_7, and R_3 and R_8, respectively, which is $\frac{1}{2}$Vcc (equivalent to *4.5 V*). $C_{static\text{-}1}$ and $C_{static\text{-}2}$ are sufficiently charged by this DC bias, thus resulting in a sustained start-up and oscillation.

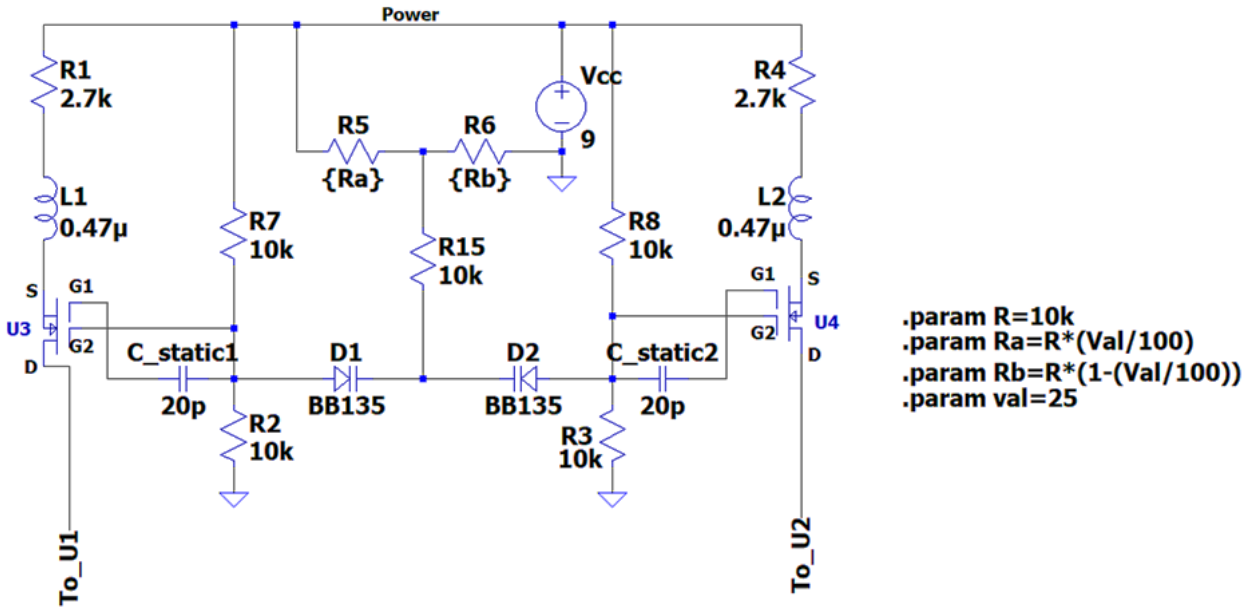

Fig. 4 Resonant circuit including loading DG MOSFETs

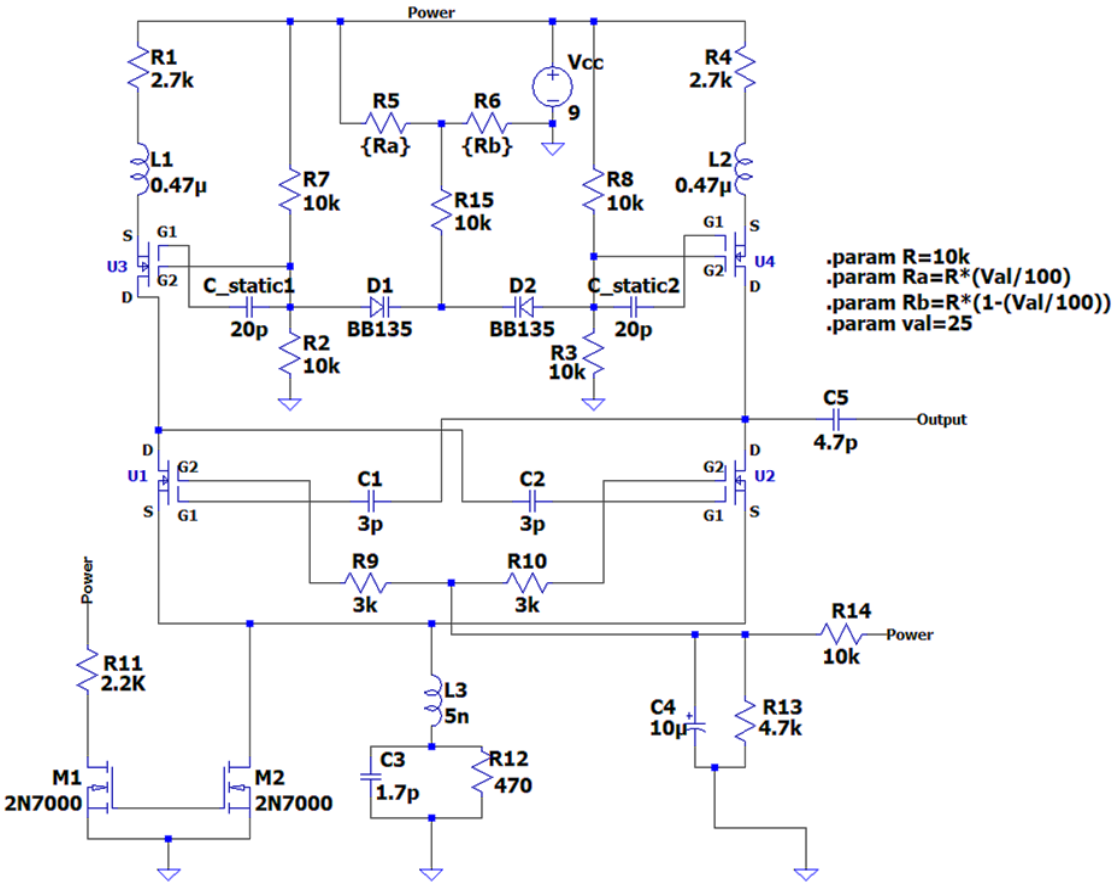

Fig. 5 Complete VCO design using active-loading differential architecture

To maintain V_S, given a drain current of 2 mA, V_S can be calculated as:

$$V_S = 5 = 9 - (2\ x\ 10^{-3}) x\ (R_1)$$

Here, $R_1 = R_4 = 2.5\ k\Omega$ (E12 value of 2.7 k to be used, as shown in Figure 4). The R1 and R4 will be used to bias both active-loading DG MOSFETs, as shown by previous study. Referring to Figure 3, the biasing of U1 and U2, is similar to the biasing of the designed VCO. Given the node labels 'To_U1' and 'To_U2' in Figure 4, these nodes will form the drain of both U1 and U2, respectively, as shown in Figure 5.

Since the resonant frequency at any point of operation is generated by U3 and U4, U1 and U2 should be adequately filtered from power supply noise and low–frequency noise from the current mirror. This will ensure odd harmonics are not coupled into the output of the VCO or add phase noise to the VCO by appearing on the tuning line of the varactors [28]. Considering second-order harmonics, the highest second harmonic is *200 MHz* (second harmonic of *100 MHz*). Thus, an RC Low-Pass Filter (LPF) can be used, with values R = *470* Ω, C = *1.7 pF*. This can be seen in R_{12} and C_3 in Figure 5. The L_3 absorbs any unwanted DC voltage from the current mirror.

As shown in Figure 5, R_5 and R_6 simulate a potentiometer, given the *.param* commands in SPICE. In the snapshot shown in Figure 5, $R_5 = 2.5\ k\Omega$ and $R_6 = 7.5\ k\Omega$. The node shown as *Power* has been used at different points in the schematic while being connected to V_{cc}, to allow the usage of one voltage source at each point in the schematic. The C_1 and C_2 are DC-blocking capacitors to prevent any unwanted DC from being injected into gate-1 of U1 and U2. R_9 and R_{10} provide pull-up to *4.5 V*, provided by the node formed R_{13} and R_{14}.

2.3. Development of Schematic Capture and PCB Design

Several design considerations were made since the proposed VCO is a low-power device operating at high frequency and susceptible to noise. The hardware design (schematic capture, PCB layout, and routing) has been performed. Specific design practices have been followed to preserve signal integrity, reduce power consumption and contribute to overall circuit robustness:

- A *9 V* regulator (Component P1 shown in Figure 6(a)) is used to provide a stable supply voltage to VCO. Other than good design practise, since there are voltage-sensitive components (varactors, potentiometers) and low-power capability is a design goal, this is essential. With the chosen regulator, there are two filter capacitors at the input and output terminal, as advised by the device datasheet [29].
- Capacitors C_6, C_7 and the inductor L_4 (shown in Figure 6(b)) have been added to the schematic as an extra level of redundancy. While the PCB footprints are not limited to being capacitors or inductors, 0805 PCB footprints were used so that a pi-filter may be added if required [30]. A pi-filter can attenuate or amplify an output signal

while matching input and output loads. This would be needed for varying loads (75 Ω coaxial connectors or RF loads). In the application and testing of the proposed VCO, L_4 will be populated with a 0 Ω resistor since the proposed VCO was designed for a 50 Ω load and will be used with a 50 Ω BNC connector.

- Power traces were routed using star-topology power distribution, i.e. thicker traces used to reduce trace impedance, routed from a single point node, with all required traces branching from the singular node. This ensures maximum power transfer and reduction of possible ripple current [32].
- A double-sided copper clad was used to etch the PCB, where one side was used as the signal plane, and the other side was used as a ground plane. This can be observed in Figure 7.

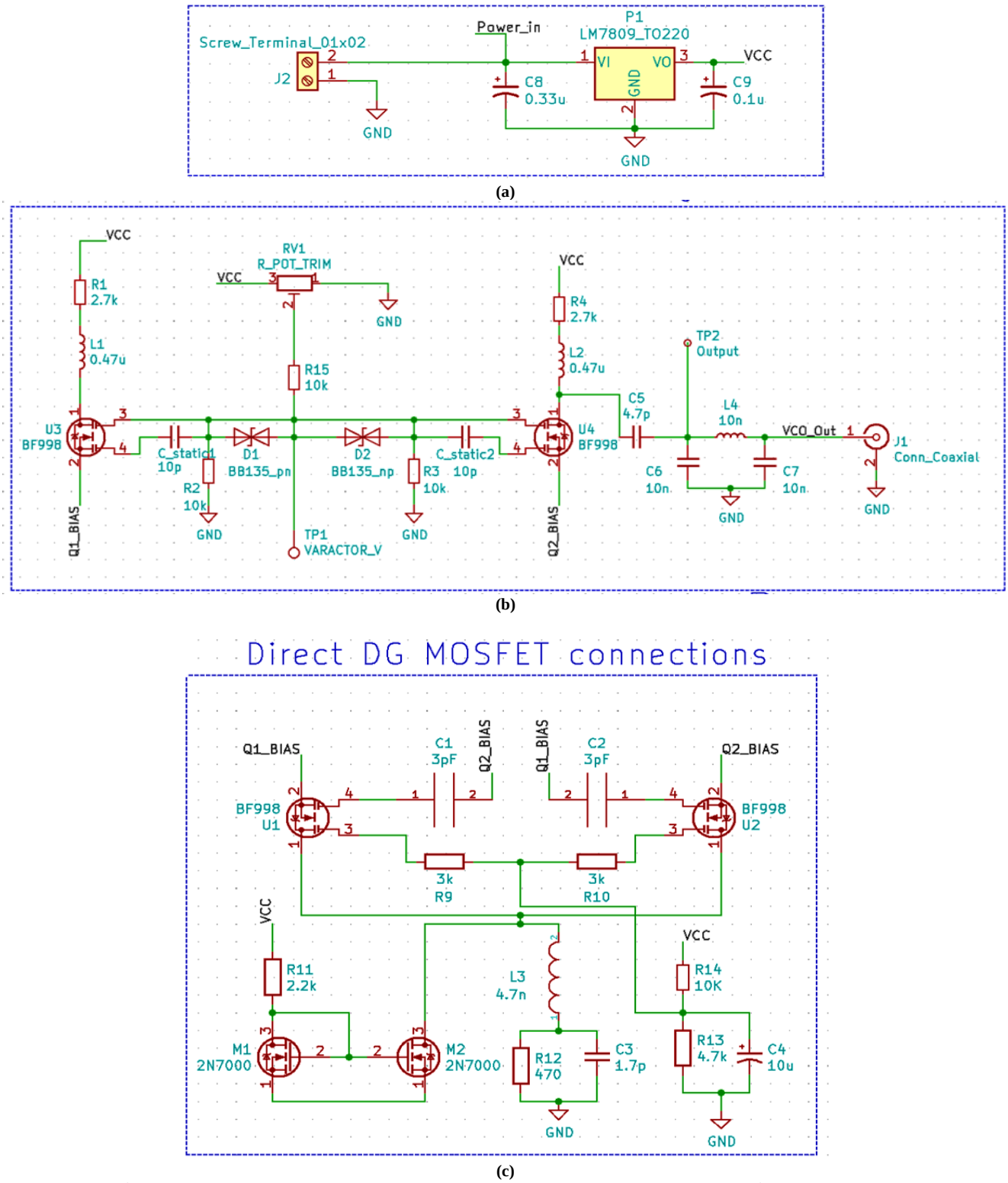

Fig. 6 Schematic for proposed VCO showing (a) Power supply section given by a 9V regulator, (b) Diode configuration and nMos current-source biasing, (c) DGMOSFET signal transistors

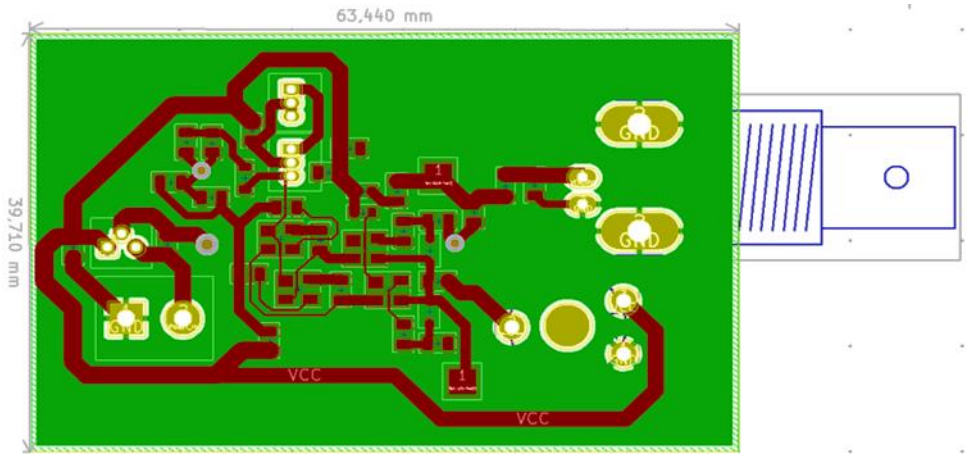

Fig. 7 The PCB layout and routing for the proposed VCO

Fig. 8 High-level block diagram of the measurement setup

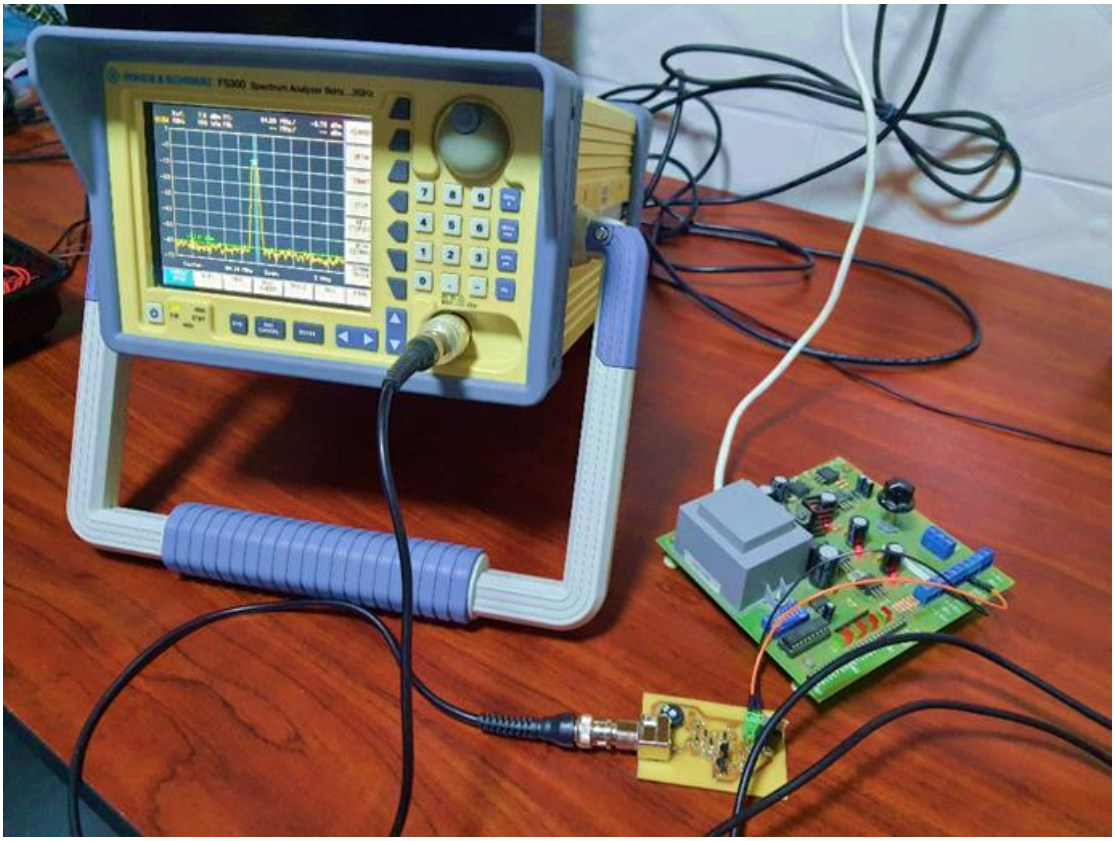

Fig. 9 Measurement setup for analysis of the designed VCO

3. Testing and Analysis of the Designed VCO

The requirement for testing an oscillator involves using a spectrum analyser, which should have a phase noise of at least 10 dB better and have a suitable dynamic range [33, 34]. The FS300 exhibits a phase noise of < -90 dBc/Hz at 10 kHz and a dynamic range of > 137 dB. In seeing this, the FS300 is sufficient to conduct the testing on the designed VCO. A high-level overview of the test setup can be seen in Figure 8, with the actual experimental setup shown in Figure 9.

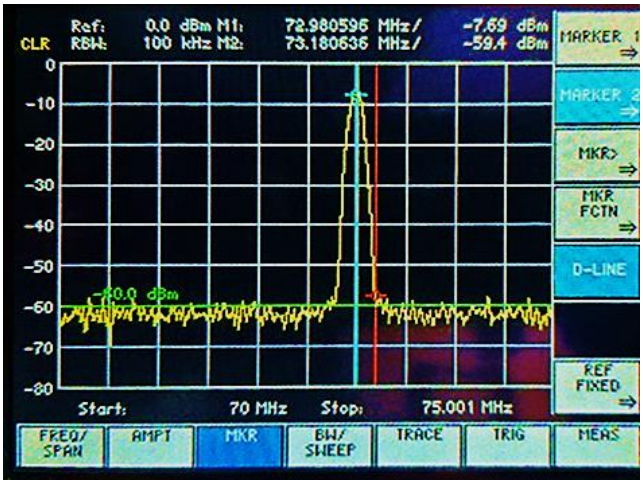

Fig. 10 Transmit power at 72.9 MHz

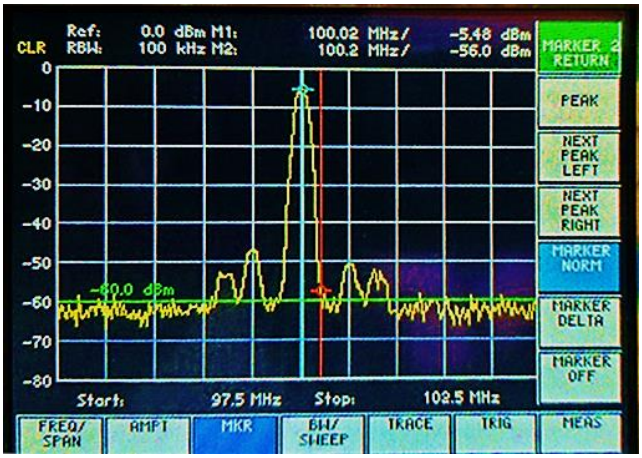

Fig. 11 Transmit power at 100 MHz

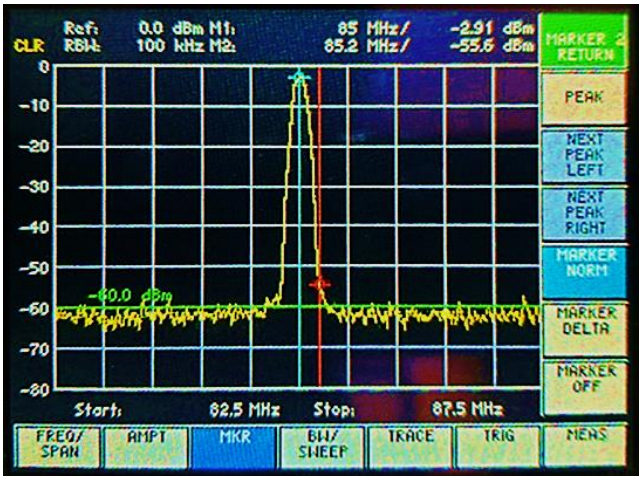

Fig. 12 Peak output power of approximately -2 dBm

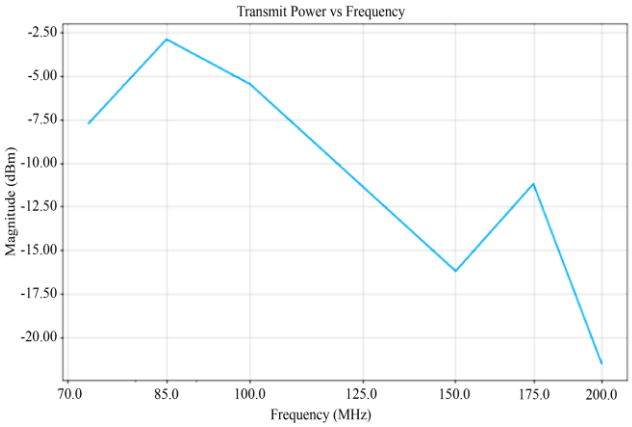

Fig. 13 Transmit power vs frequency for tuning range

3.1. Output Power

The output power of a fully-fledged VCO from APITech [35] ranges from *7 – 10 dBm* minimum. These VCOs typically include amplifiers and buffer circuitry, increasing output power [36]. In the designed VCO, neither a buffer nor a Darlington configuration was used to drive the load. The transmit power was measured for the frequency range of *70 – 200 MHz* (this includes the second harmonic of the tuning range, i.e. 70 – 100 MHz). The transmit power at *73 MHz* can be seen in Figure 10, which is *-7.69 dBm*, shown by the blue marker. At the furthest end of the spectrum (excluding the second harmonic), the transmit power at *100 MHz* is *-5.48 dBm*, as shown in Figure 11. The maximum output power of *-2.91 dBm* is shown in Figure 12.

Following further results of the tuning range of *70 – 100 MHz*, which includes the transmit power of the second harmonic, these results are depicted in Figure 13. A clear degradation is observed for frequencies above the tuning range, i.e. frequencies greater than *100 MHz*. This can be improved by adding an output buffer or using conventional methods to improve the phase noise at these frequencies. These may include a decrease in the tuning voltage gain K_{VCO}. The tuning voltage gain is determined by the ratio of frequency to voltage. Reducing this would entail increasing the supply voltage, as shown by *Hsu et al.* [35], where an increase of power dissipation from *3 mW* to *5 mW* yields a phase-noise improvement of approximately *85 dBc/Hz*. Replacement of the current mirror with a full cascode output stage, as implemented by [13], will reduce the amount of noise coupled into the output. Table 1 summarises the output power in dBm and $V_{pk\text{-}pk}$, depicted in Figure 13.

Table 1. Frequency vs Power (dBm, $V_{pk\text{-}pk}$)

Frequency (MHz)	Output Power (dBm)	Output Voltage ($V_{pk\text{-}pk}$)
73	-7.74	0.26
85	- 2.91	0.45
100	-5.48	0.37
150	-16.2	0.098
175	-11.2	0.17
200	-21.5	0.053

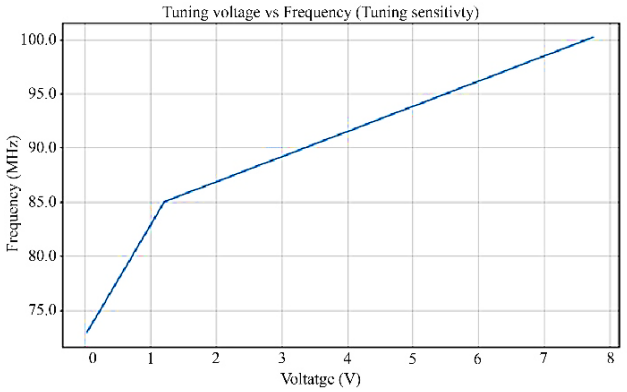

Fig. 14 Tuning sensitivity for proposed VCO

3.2. Tuning Sensitivity

A VCO's tuning range is determined by its resonant circuit's collective inductance and capacitance. As designed in the proposed VCO, varactor diodes are used to provide a variable capacitance. The voltage of this resonant circuit determines the efficiency, power consumption, and linearity of the VCO's operation [37]. The formula to compute the tuning sensitivity for a tuning range is:

$$K_{VCO} = \frac{\omega_2 - \omega_1}{V_2 - V_1} \quad (6)$$

Where ω_1 and ω_2 are oscillating frequencies, and V_1 and V_2 are the corresponding voltages of the resonant circuit outputs/varactor diodes output junction. The tuning sensitivity of the proposed VCO is depicted in Figure 14.

For the tuning range of 73 MHz – 85 MHz, given Equation 6, the tuning sensitivity KVCO is approximately 10.23 MHz/V. For the tuning range of 85 MHz – 100 MHz, KVCO is 2.3 MHz/V.

3.3. Oscillator Phase Noise (PN)

As discussed, the PN of a VCO determines its spectral purity and immunity to noise coupled into the circuit for "x" Hz away from the oscillating frequency, where "x" is a frequency offset. The phase noise from a source can be caused by a number of factors, e.g. internal noise of varactor diodes, power supply noise, inherent noise of the semiconductors used, etc. [37].

3.3.1. Frequency Offsets from a Single Oscillating Frequency

The phase noise for a VCO can be assessed by specified offsets to characterise the noise in the oscillating frequency. *Balogun et al.* [38] have shown the degradation of optical transmission systems, given carrier frequency offsets in phase noise estimation.

Figure 15 shows the importance of measuring the phase noise at different offsets, as the phase noise level should ideally follow the profile shown, from an initial offset of *10 Hz* to *10 MHz*, which should resemble the noise floor of the VCO. This form of phase noise is also known as discrete phase noise [9] and is given by:

$$\text{Phase Noise}_{(\text{Discrete})} = P_{(\text{Carrier})} - P_{(\text{Carrier} \pm \text{frequency offset})} \quad (7)$$

Where $P_{(\text{Carrier})}$ is the power of the carrier signal in dBm, and $P_{(\text{Carrier} \pm \text{frequency offset})}$ is the power of the carrier signal that is shifted by an offset. The continuous phase noise of the output signal can also be approximated using the discrete bandwidth, which is the phase noise per *1-Hz* bandwidth and is dependent on the carrier's resolution bandwidth (RBW) and carrier offset.

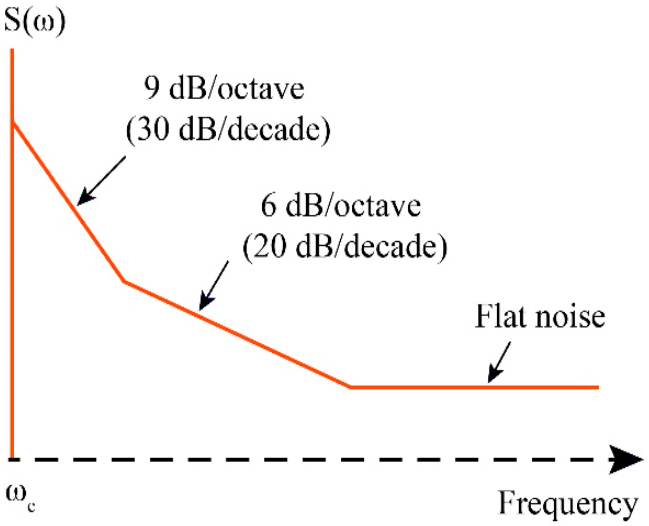

Fig. 15 Typical phase-noise profile for a VCO [15]

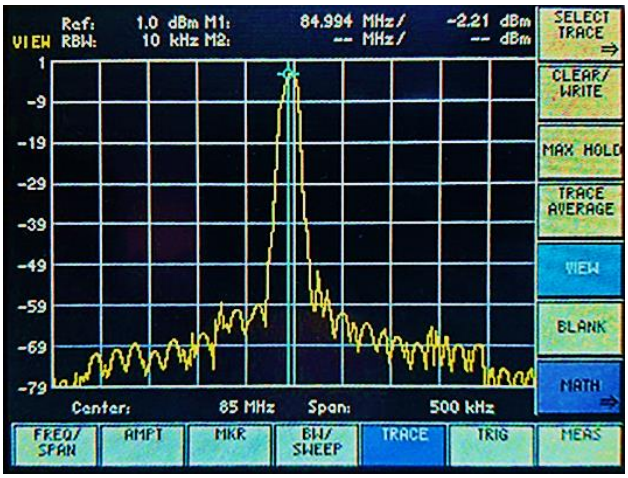

Fig. 16 Carrier ≈ 85 MHz, output power = - 2.21 dBm, RBW = 10 kHz

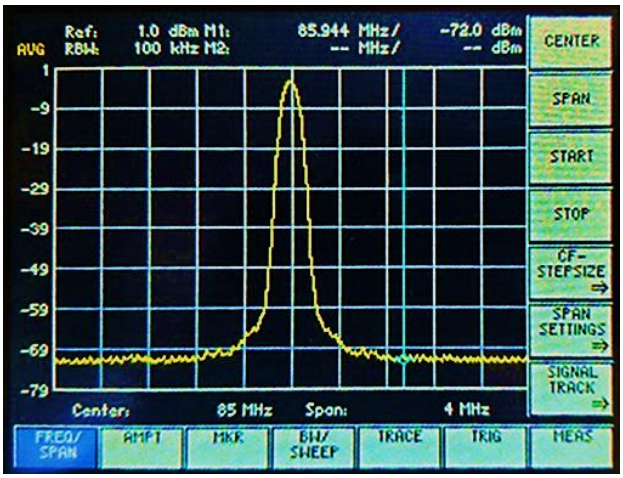

Fig. 17 Carrier ≈ 86 MHz, showing an output power = -72.0 dBm, RBW = 100 kHz, carrier offset = 1 MHz

The RBW is proportional to the bandwidth of the signal. As shown in Figure 16 and Figure 17, the RBW of the signal is *10 kHz* and 1*100 kHz*, shown in the top-left of the analyser's screen. To compute the continuous phase noise:

$$\text{Phase Noise}_{(\text{Continuous})} = \text{Phase Noise}_{(\text{Discrete})} - 10\log(\text{RBW}) \quad (8)$$

Thus, for PN(Discrete), the continuous phase noise PN(Continuous) can be defined as the PN in a 1-Hz bandwidth at the same offset used to compute PN(Discrete). The test results for the discrete (PN(D)) and continuous phase noise(PN(C)) measurements can be seen in Table 2 and Table 3, given the RBW used, output power P_o and carrier offset.

Table 2. Test results for discrete phase noise vs Carrier offset

		f_o + 10 kHz		f_o + 100 kHz		f_o + 1 MHz	
f_o (MHz)	**P_o (dBm)**	**P_o (dBm)**	**PN(Discrete) (dBc/Hz)**	**P_o (dBm)**	**PN(Discrete) (dBc/Hz)**	**P_o (dBm)**	**PN(Discrete) (dBc/Hz)**
85 (84.994)	-2.21	-4.88	-2.67	-67.5	-65.29	-72	-69.79
170 (169.98)	-10.2	-18.4	-8.2	-76.3	-66.1	-71.9	-61.7

Table 3. Test results for continuous phase noise vs Carrier offset

		f_o + 10 kHz (RBW = 10 kHz)		f_o + 100 kHz (RBW = 10 kHz)		f_o + 1 MHz (RBW = 100 kHz)	
f_o (MHz)	**P_o (dBm)**	**PN(D) (dBc/Hz)**	**PN(C) (dBc/Hz)**	**PN(D) (dBc/Hz)**	**PN(C) (dBc/Hz)**	**PN(D) (dBc/Hz)**	**PN(C) (dBc/Hz)**
85 (84.994)	-2.21	-2.67	-42.67	-65.29	-105.29	-69.79	-119.79
170 (169.98)	-10.2	-8.2	-48.2	-66.1	-106.1	-61.7	-111.7

*f_o is the fundamental/oscillating frequency

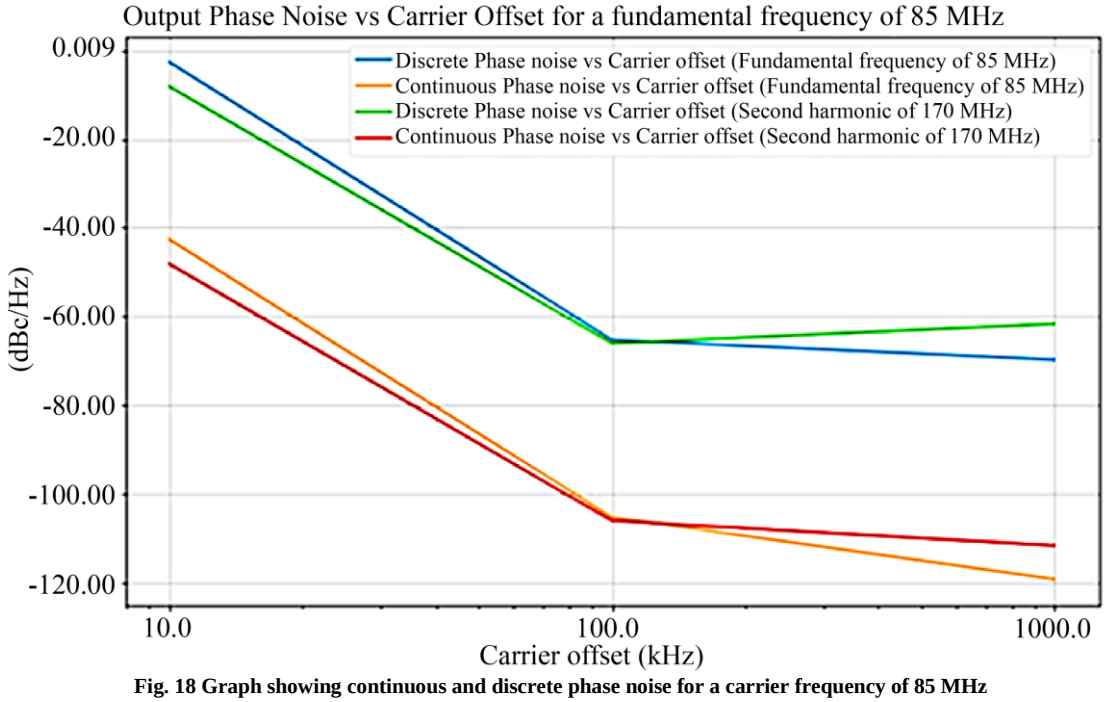

Fig. 18 Graph showing continuous and discrete phase noise for a carrier frequency of 85 MHz

3.3.2. Singular Frequency Offset for the Entire Tuning Range

A singular frequency offset of 200 kHz was chosen for this measurement, and the phase noise was manually measured. The tuning range of the oscillator is *30 MHz (70 – 100 MHz)*; thus, an offset < 1% of the tuning range was chosen for granularity. For a frequency offset of ±*200 kHz*, the phase noise was measured for the tuning range of the VCO and the subsequent second harmonics. The phase noise for *73.1 MHz – 200 kHz (which is 72.9 MHz)* and *100 MHz + 200 kHz (100.2 kHz)* was measured to be - *51.71 dBc/Hz* and - *50.52 dBc/Hz*, respectively. A summary of the results can be seen in Table 4, and the comprehensive testing for phase noise vs carrier offset can be seen in Figure 18, followed by the phase noise over the frequency range in Figure 19.

Table 4. Phase noise for the proposed VCO

		f_o – 200 kHz		f_o + 200 kHz	
Fundamental Frequency f_o (MHz)	**Output power P_o (dBm)**	**Output Power (dBm)**	**Phase Noise (dBc/Hz)**	**Output Power (dBm)**	**Phase Noise (dBc/Hz)**
72	-7.69	-57.2	-49.51	-59.4	-51.71
85	-2.91	-56.6	-53.69	-55.6	-52.69
100	-5.48	-56.2	50.72	-56	-50.52
The second harmonic of the tuning range					
150	-16.2	-61.1	-44.9	-57.3	-41.1
175	-11.2	-55.4	-44.2	-50.6	-39.4
200	-21.1	-59.2	-38.1	-60.4	-39.3

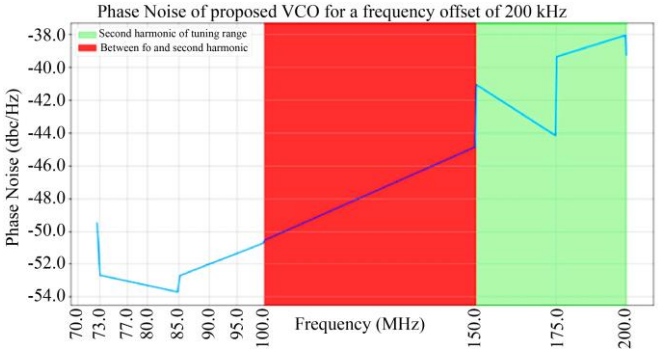

Fig. 19 Phase noise computation for the proposed VCO for the designed tuning range and second harmonic

From the measurement of the phase noise of the VCO, observations can be made about its performance at high frequency and noise immunity. In section 3.3.1, the classical definition for the phase noise of a VCO was followed, given by cited works, i.e. the power of a signal at a carrier offset (typically each decade) was subtracted from the power of the carrier itself. The computation was done manually using markers provided by the spectrum analyser.

Given the highest transmit power, the carrier frequency of *85 MHz* should exhibit the lowest phase noise for the entire tuning range [15]. This is possibly attributed to a higher Q-factor occurring at this resonant frequency [18] and the reduction in the overall on-resistance of U3 and U4, given the inductance and capacitance of the LC resonator circuit (shown in Figure 4) [20]. In section 3.3.2, a singular carrier offset of *200 kHz* was used to allow computation of the phase noise for the entire tuning range *(70 – 100 MHz)*, which is provided by the designed VCO, and not a single fundamental frequency.

As expected, PN increases as the fundamental frequency increases for the tuning range only. A high-phase noise can be observed at the end of the tuning range (for the fundamental frequency and its corresponding second harmonic). Using Figure 15 as a reference, the proposed VCO achieves *-2 dBm/decade* for a *10 kHz* offset, then < *-60 dBc/Hz* for a *100 kHz* carrier and above [40-43], as shown in Figure 18. This is favourable at high frequencies, as the signal's noise floor resides at a low power level.

3.4. Figure of Merit (FOM) and Tuning Figure of Merit (FOM_T)

While considering all aspects (phase noise, bandwidth of oscillating frequency, and power consumption), the FOM provides a comprehensive performance index for tuning oscillators. The FOM [26] can be approximated by:

$$\text{FOM} = \text{PN} - 20\cdot\log10\left(\frac{f_c}{\Delta f}\right) + 10\cdot\log10\left(\frac{P_{DC}}{1\ mW}\right) \quad (9)$$

where f_c is the oscillating/centre frequency, Δf is the carrier offset, and P_{DC} is the power consumption. It is appropriate to evaluate the FOM at a centre frequency of 85 MHz, given the power consumption is at its peak, as peak output power is provided at this frequency. The FOM can be visualised in Figure 20 for similar carrier offsets used to compute the phase noise in section 3.3.1. The FOM_T is the resultant tuning FOM, which would include the entire tuning range, using the FOM as a reference [27]. The FOM_T can be given by:

$$\text{FOM}_T = \text{PN} - 20\cdot\log10\left(\left(\frac{f_c}{\Delta f}\right)\cdot\frac{TR\%}{10}\right) + 10\cdot\log_{10}\left(\frac{P_{DC}}{1\ mW}\right) \quad (10)$$

Using a carrier offset of *1 MHz* and the oscillating Frequency of *85 MHz*, P_{DC} can be approximated as peak power consumption (*36 mW*). The TR = 35% is the percentage of the difference in voltage of varactor diode junctions between *85 MHz* and *86 MHz*. Here, the FOM_T is approximately *-126.76 dBc/Hz* for a *1 MHz* carrier offset using Equation 10.

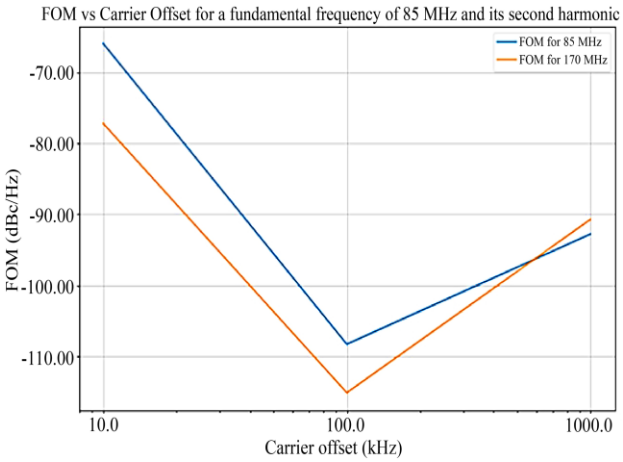

Fig. 20 FOM vs Carrier frequency for a fundamental frequency of 85 MHz

3.5. Summary of Proposed VCO Specifications and Comparative Analysis

The resultant specifications for the designed VCO and its HW implementation are shown in Table 5. A further comparative summary is performed in Table 6, from all noted literature. The comparison is done between common parameters of interest.

Table 5. Results of testing and analysis of the hardware implementation of the proposed VCO

Parameter	Test Results of HW Implementation
Tuning range	73 – 100 MHz
Output power	36 mW
Voltage supply	9V
Tuning gain	10.23 MHz/V (73 – 85 MHz); 2.3 MHz/V (85 – 100 MHz)
Discrete Phase noise (best for tuning range, occurring at 85 MHz, 1 MHz offset)	-69.79 dBc/Hz
Continuous Phase noise (best for tuning range occurring at 85 MHz, 1 MHz offset)	-119.79 dBc/Hz
Phase noise (best for the second harmonic, occurring at 170 MHz, 100 kHz offset)	-66.1 dBc/Hz
Continuous Phase noise (best for second harmonic occurring at 170 MHz, 1 MHz offset)	-111.7 dBc/Hz
FOM	-92.82 dBc/Hz
FOMT	-126.76 dBc/Hz

Table 6. Comparison of the different design techniques with this work

VCO designed	Tuning Range	Output Power	Phase Noise*	FOM*	Power Consumption
Widely Tunable K-band [8]	18.2 GHz – 23.28 GHz	- 1.35 dBm	-105 dBc/Hz (1 MHz)	-179 dBc/Hz (1 MHz)	24 mW, given a supply current of 24 mA and supply voltage of 1V
90nm Push-push Dual-band Cross-coupled [10]	26.38 GHz-28.15 GHz; 52.76 GHz - 56.30 GHz	-37dBm	-108.57 dBc/Hz and -98.43 dBc/Hz for each tuning range, respectively	-108.57 dBc/Hz; -98.43 dBc/Hz (10 MHz)	-
Low Power, High-Speed Differential Amplifier Ring [11]	87 – 910 MHz	-	-	-	3.11 mW
Fundamental VCO with integrated output buffer [12]	117.5 – 121.5 GHz	3dBm at peak	-93.3 dBc/Hz (1 MHz)	-	1.86 W (310 mA from a 6 V power supply)
Colpitts VCO [13]	3.59 – 3.69 GHz	-5 to -5.1 dBm	-130.1 to -129.1 dBc/Hz (1 MHz)	-183.9 dBc/Hz (1 MHz)	56 mW (11.2 mW at 5 V supply)
Noise-shifting Colpitts [13]	3.58 – 3.67 GHz	-2.5 to -3.5 dBm	- 132.4 to – 130.2 dBc/Hz (1 MHz)	-186.3 dBc/Hz (1 MHz)	54 mW (10.8 mA at 5 V supply)
Fabricated Darlington-based class-C [13]	2.76 – 2.91 GHz	-3.06 dBm to -4.18 dBm	- 138.6 to- 135.9 dBc/Hz (1 MHz)	-191.2 dBc/Hz (1MHz)	47.5 mW (9.5 mA at 5 V supply)
This Work	73 – 100 MHz; 140 - 200 MHz	-7.74 dBm to -2.91 dBm; -21.5 dBm to -5.44 dBm	-69.79 dBc/Hz (1 MHz offset)	-92.82 dBc/Hz (1 MHz)	36 mW (4 mA at 9V supply)

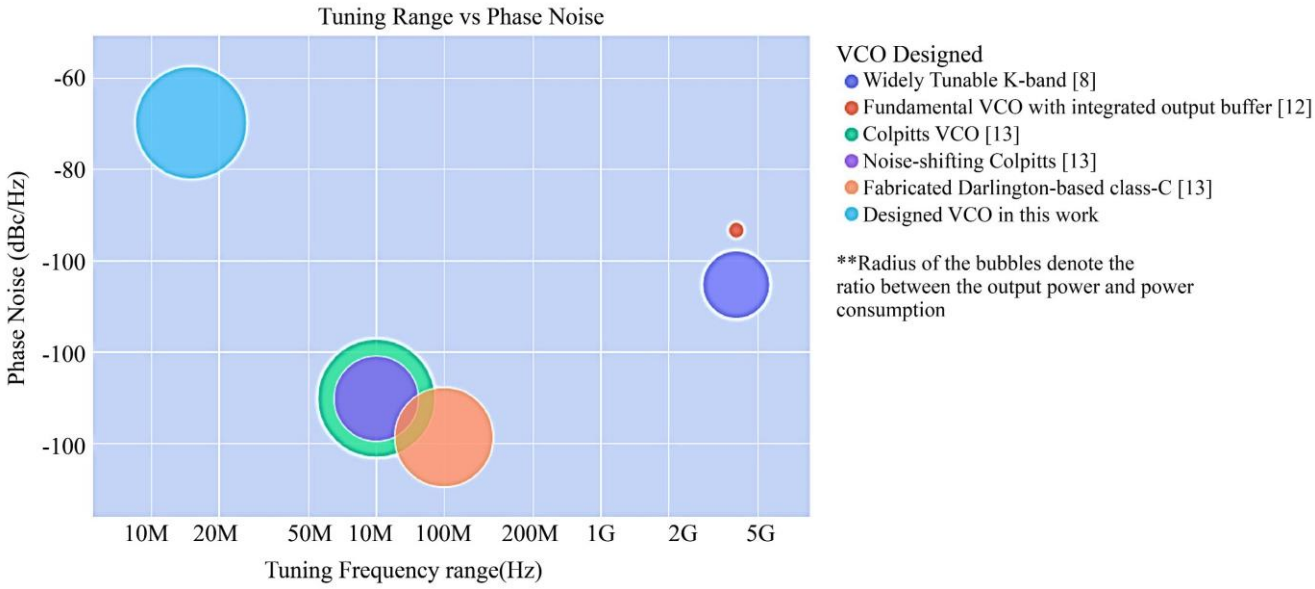

Fig. 21 Analysis of the tuning range and phase noise

Given Table 6, Figure 21 denotes the analysis and the graphical relationship between the tuning range and phase noise for the noted literature. The use of an output stage has been shown to improve the phase noise for VCOs with a larger tuning range than the designed VCO, given that the referenced literature all exhibit a lower phase noise. However, the addition of such output stages degrades the output power relative to the power consumption and resulting power efficiency (given by the radius of each bubble in Figure 21).

4. Conclusion and Future Recommendations

The designed VCO and its design process have been defined to achieve the output power while employing measures for noise suppression, such as filtering and optimal PCB design measures. As noted in the functional specifications, the output power was designed to be *-2 dBm* at peak, which is approximately *500 mV*$_{pk\text{-}pk}$. This has been achieved (as in Figure 12) at *85 MHz*. The Q-factor of the VCO is the highest at this frequency. For the tuning range of *70 – 100 MHz*, the output power ranges between *-7.74 dBm* and *-2.91 dBm*. This translates to an output of *200mV*$_{pk\text{-}pk}$ *– 500 mV*$_{pk\text{-}pk}$. This has met the functional specifications outlined for the design of the VCO. Given this output power, the proposed VCO aligns with the relevant literature, as the comparative study shows.

The tuning sensitivity of the proposed VCO can be improved by choosing an alternative varactor diode. Given hindsight, the need arises as the low tuning sensitivity of the 85 – 100 MHz tuning range can be improved. The varactor diode and resonant circuit are adequate for providing a full tuning range. An abrupt diode may be used to find an alternative to the hyperabrupt diode used in the proposed VCO. The abrupt diode provides a larger tuning range (*0 – 60 V*, compared to the tuning range of the hyperabrupt diode, which is approximately *0 – 20 V*). An abrupt diode can provide a higher Q, reducing the phase noise coupled to the output by the varactor diode.

The oscillator's phase noise was measured extensively, providing insight into the noise level at different oscillating frequencies and frequency offsets. The designed VCO exhibits its best discrete PN *of -69.79 dBc/Hz at 85 MHz*, at a carrier offset of *1 MHz*. The phase noise can be improved given the cited works in Table 5. A method to improve the phase noise is to include a low-noise buffer for the specified application.

The buffer can prevent unnecessary current-sinking from the oscillator's output. Several considerations must be made when designing a buffer, such as impedance matching (which provisions were made for in the schematic design for the proposed VCO) and noise reduction techniques (filtering of low-frequency noise). To further reduce the phase noise, replacing the varactor diode can be considered to potentially provide more capacitance in the resonator circuitry. Given a power supply voltage of *9 V* and a nominal drain current of *4 mA*, the power consumption of the proposed VCO is *36 mW*. The output power produced by the VCO indicates better power efficiency to cited works.

From the analysis of the designed VCO and design constraints imposed, the VCO can maintain a better FOM of -92.82 dBc/Hz, given a dual-band output and can be greatly improved by simple additions to the design. From the cited works, which include the measures of providing low power consumption, the proposed VCO performs better in this regard, with a larger supply voltage and lower power consumption. This contributes to better power efficiency. This shows that the active-loaded differential topology, coupled with the DG MOSFET, can provide a high output power for lower noise production.

Applications would be able to tailor the designed VCO to their specification and improve their system, which has also been made easier by adding the pi-filter in the PCB design. In addition to this, in the future, various materials, such as high-k dielectrics material, can be used in addition

to different MOSFET structures, such as the CSDG MOSFET.

Frequency pushing and load pulling are further investigations to be completed in this work, which requires the schematic to be re-designed partially to accommodate the absence of a 9 V regulator (this would be removed to provide a comprehensive analysis, allowing the supply voltage to fluctuate naturally), addition of the pi filter and output buffer. The designed VCO could also be improved by using an abrupt varactor diode, further investigating the tuning characteristic and resulting phase noise.

Author Contributions

Suvashan Pillay and Viranjay M. Srivastava conducted this research; Suvashan Pillay designed and analyzed the model with data and wrote this article; Viranjay M. Srivastava has verified the result with the designed model; all authors approved the final version.

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Data Availability Statement

All data and materials used to prepare this manuscript are available in this document.

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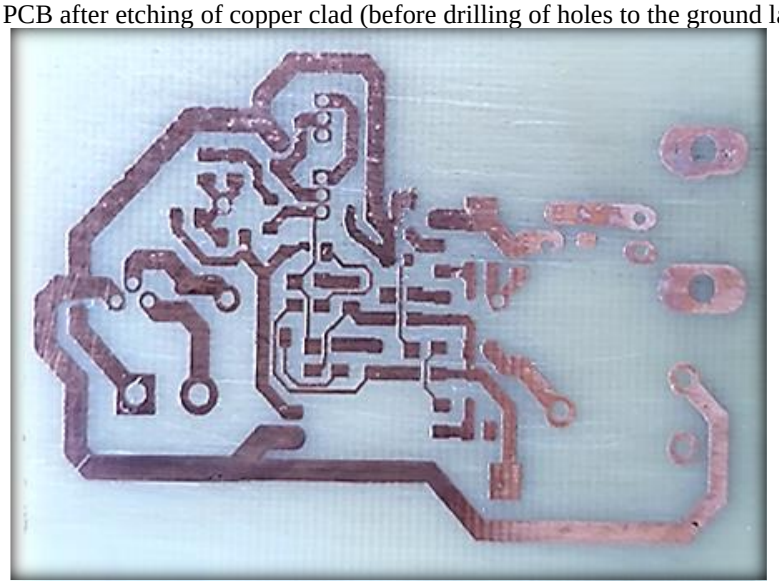
Appendix 1

Bare PCB after etching of copper clad (before drilling of holes to the ground layer)



Populated PCB (soldered components, soldered vias to connect up-side to bottom-side GND)