

Article

Enhanced Voltage Balancing Algorithm and Implementation of a Single-Phase Modular Multilevel Converter for Power Electronics Applications

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Abstract

This paper presents an innovative primary control strategy for a modular multilevel converter aimed at enhancing reliability and dynamic performance for power electronics applications. The proposed method utilises interactive modelling tools, including MATLAB Simulink (2022b) for algorithm design and Typhoon HIL (2023.2) for real-time validation. The circuit design and component analysis were carried out using Proteus Design Suite (v8.17) and LTSpice (v17) to optimise the hardware implementation. A power hardware-in-the-loop experimental test setup was built to demonstrate the robustness and adaptability of the control algorithm under fixed load conditions. The simulation results were compared and verified against the experimental data. Additionally, the proposed control strategy was successfully validated through experiments, demonstrating its effectiveness in simplifying control development through efficient co-simulation.

Keywords: capacitor voltage balancing; hardware-in-the-loop simulation; modular multilevel converters; pulse width modulation; typhoon



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1. Introduction

Power electronic converters are crucial for the effective operation of renewable energy, automotive, and other modern industrial processes, where they facilitate the conversion, control, and management of electrical energy [1]. However, as modern power systems become more complex in their operation, traditional converter topologies such as the two-level inverter encounter limitations such as large switching losses, high operating frequency, power devices rating constraints, etc., that deteriorate the efficiency of this inverter, especially under dynamic conditions [2]. To overcome these challenges and latching upon the advancements in power electronic semiconductor devices, academia and industry developed the concept of multilevel inverters (MLIs) [3,4].

MLIs offer several advantages over traditional two-level inverters, including high-quality output waveforms, reduced voltage stress on power switches, redundancy in switching states, increased power quality, and minimised harmonic distortion, which reduces or eliminates the need for output filter circuitry [5–8]. MLIs are widely applied in various fields such as renewable energy conversion, high-voltage DC transmission, motor drives, and powertrain applications. However, significant drawbacks of this class of

inverter include the large number of switching devices, which lead to circuit complexity and increased costs, especially as the number of levels increase, in addition to complexity in the control method [6,8].

Typical multilevel inverters discussed in the literature include the neutral point clamped (NPC) [9], cascaded half bridge (CHB) [10], flying capacitor (FC), and the modular multilevel converter (MMC) [11,12]. While each of these MLIs presents unique advantages over each other, the MMC has gained particular interest in recent years due to its unique structure, scalability, modularity, fault-tolerant operation, and reliability [13]. Moreover, the MMC is preferred for high power transmission, offering practical applications for renewable energy integration. However, despite these advantages, the problem remains of its complex control structure and complicated circuitry common to MLIs.

The MMC offers significant advantages for high-power applications, including scalability, low harmonic distortion, and a modular structure. However, these benefits come with increased control complexity due to the need to manage numerous submodules, each containing a capacitor that requires precise regulation. Key control challenges include balancing capacitor voltages across submodules, managing circulating currents, coordinating the switching of multiple devices, and ensuring overall system stability [14]. Among these, maintaining capacitor voltage balance is critical, as any imbalance can degrade performance, increase losses, and even lead to system failure.

To ensure efficient and reliable operation of the MMC, the submodule capacitors must be balanced. This voltage-balancing control problem has been addressed in various examples of the literature [13,15–18]. The common method of balancing the capacitor's voltage involves the use of sorting algorithms. Popular algorithms include the bubble sort, which has been modified in [19] using a brute force methodology. Despite its ease of implementation, the bubble sort struggles with handling large data sets, leading to increased computational effort and reduced efficiency, especially in real-time applications where swift control responses are crucial. Another approach presented in [20] uses a modified mapping strategy based on the min/max method, which provides a quasi-sorted list applicable to any number of MMC levels. While effective, this method still faces challenges in terms of computational complexity and scalability in higher-level systems. It is important to note that the choice of voltage balancing algorithm is closely tied to the modulation technique employed.

Phase-shifted PWM (PS-PWM) is widely used for submodule balancing due to its even switching distribution, but it often results in higher capacitor ripple than nearest-level modulation (NLM) [21,22]. NLM simplifies balancing but can increase voltage dispersion, while hybrid predictive and radix-based sorting schemes reduce ripple at the cost of significant computational effort [23,24]. Building on these efforts, this work introduces a modified quick-sort algorithm with dynamic pivot selection and adaptive sorting depth, reducing redundant comparisons and improving scalability. Unlike earlier methods, the approach is validated in real time on Typhoon HIL402, demonstrating both novelty and practical feasibility.

While developing advanced control strategies for MMCs is crucial, validating these strategies in real-world conditions remains a significant challenge. The existing literature often focuses on simulation-based validation of MMCs, leaving gaps in empirical validation and real-time hardware implementation. For instance, refs. [18,25,26] presented detailed simulation models for MMCs, offering valuable insights into control strategies and system behaviour. However, these studies lack the experimental validation necessary to confirm real world performance, which is critical for high-power applications. Although these simulations provide a comprehensive understanding of MMC control under ideal conditions, they do not address the challenges associated with real-time hardware implementation and

testing. Such challenges, including timing issues, switching delays, and interactions with physical components, are crucial for ensuring reliable and robust performance in practical MMC applications.

Existing studies have primarily relied on platforms such as DSpace [27], OPAL-RT [28], and Texas Instruments [29] for the simulation and validation of MMC control strategies. All these platforms offer robust simulation environments but often fall short in replicating the real-time, hardware-specific challenges encountered in practical applications. For instance, the latency, switching delays, and noise that occur in real hardware can significantly impact the performance of MMCs—factors that are often overlooked or underestimated in purely software-based simulations.

In response to these limitations, co-simulation techniques have gained traction in recent years. Co-simulation enables the integration of multiple simulation platforms, allowing different subsystems of the MMC to be modelled and tested simultaneously [30,31]. For example, electrical circuits can be simulated in MATLAB/Simulink (2022b), while control algorithms are tested in OPAL-RT, allowing researchers to evaluate system performance in a more comprehensive manner. However, despite the benefits of co-simulation in handling the complexity of MMCs, it still does not fully address the challenges of real-time hardware validation. The gap remains in capturing the real-world dynamics, such as timing mismatches and the impact of physical hardware components on control performance.

To bridge this gap, hardware-in-the-loop (HIL) systems have emerged as a powerful solution. HIL platforms combine real-time simulation with actual hardware components, enabling comprehensive testing of control strategies in environments that closely mimic real-world conditions. However, when it comes to multilevel inverters, researchers often avoid power hardware-in-the-loop (P-HIL) validation. This is mainly due to the potential risks involved in directly connecting the multilevel inverter to physical power components, such as motors or energy storage devices. Additionally, the insufficient control of high voltage and power levels can result in safety hazards, including electric shock, equipment damage, and other risks.

Several HIL validation implementations for MLIs are found in the literature. For example, ref. [32] validated a modified CHB inverter using the DSPACE platform, highlighting the ease of implementation but noting that the control complexity is less than that of MMCs. Similarly, ref. [33] used RT Box1 by PLEXIM for rapid prototyping and testing of an NPC-based multilevel inverter. In [34], the NI PXI co-simulation system was utilised to investigate the stability metrics of an islanded three-level inverter-based microgrid. Additionally, ref. [35] employed power HIL to validate an interface algorithm for testing smart transformers, demonstrating the effectiveness of HIL in replicating real-world conditions for advanced power electronics systems. However, despite the success of these approaches, most HIL platforms remain prohibitively expensive, particularly for researchers in developing countries where access to adequate funding may be limited. This cost barrier hinders wider adoption of HIL for real-time validation, limiting opportunities for empirical testing in regions where resources are constrained.

Recent studies have continued to explore capacitor balancing in MMCs, including AI-based predictive strategies, hybrid modulation schemes, and clustered average-value models to reduce computational cost [36]. While these approaches have shown promise, they often lack real-time hardware validation or remain limited by increased algorithmic burden when scaled to higher submodule counts. Furthermore, balancing methods based on sequential allocation or fixed pivot sorting still face challenges of redundant comparisons, tie-related errors, and limited scalability.

To address these gaps, this work proposes a modified quick-sort-based algorithm for capacitor voltage balancing that combines dynamic pivot selection with adaptive sorting

depth. This innovation reduces unnecessary comparisons, mitigates tie-related instabilities, and demonstrates scalability to larger MMC configurations. Importantly, the method is validated in a power hardware-in-the-loop (PHIL) environment using a three-level MMC prototype, thereby capturing real-world switching dynamics that purely simulation-based studies overlook. The novelty of this work therefore lies in uniting an efficient, scalable sorting strategy with experimental PHIL validation, providing a practical pathway toward reliable large-scale MMC control.

The remainder of this article is organised as follows: Section 2 presents the working principle of the MMC converter system, including its mathematical modelling and switching signal generation strategy and the hardware implementation of the converter prototype. Section 3 discusses the simulation and experimental results used to validate the proposed approach. Section 4 concludes the paper and outlines potential directions for future research.

2. Materials and Methods

This section outlines the methodology adopted for the design, modelling, and implementation of the half-bridge modular multilevel converter (MMC) configuration. It describes the working principle, mathematical modelling, and switching signal generation based on the Level-Shifted Pulse Width Modulation (LS-PWM) technique. The control logic was initially developed and evaluated in MATLAB/Simulink (2022b), where the switching algorithm and capacitor voltage balancing strategy were implemented using LS-PWM. The validated controller was then automatically exported as C code and integrated into the Typhoon HIL platform for real-time simulation and hardware-in-the-loop (HIL) testing. This workflow ensured a seamless transition from offline simulation to real-time control evaluation.

2.1. Working Principle of MMC

The modular multilevel converter (MMC) is composed of cascaded submodules (SMs) connected in series to form the upper and lower arms of each phase leg, as shown in Figure 1. In this work, each submodule adopts a half-bridge configuration consisting of two IGBTs and one capacitor. By appropriately inserting or bypassing the SM capacitor, discrete voltage levels are synthesised at the converter terminal, enabling the formation of a staircase AC output waveform [14].

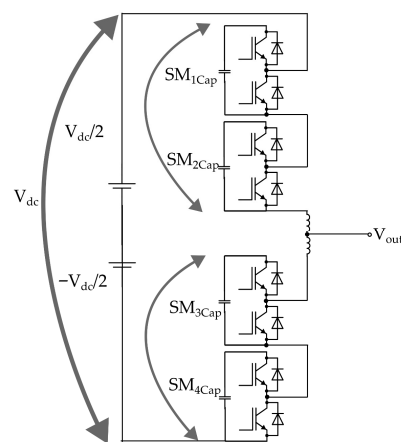


Figure 1. Three-level half-bridge modular multilevel converter setup.

The overall configuration of the 3-level half-bridge MMC leg investigated in this work is shown in Figure 1. Each arm is composed of two series-connected submodules ($N = 2$), an arm inductor, and a resistance. The midpoint of the two arms forms the AC terminal

connection to the load, while the common DC-link voltage V_{dc} provides the input supply. This leg-level schematic establishes the structural basis of the converter used in this study.

This modular structure allows scalability, as increasing the number of SMs improves the quality of the output voltage and reduces harmonic distortion. However, the way in which the SMs are energised is a key distinction between different multilevel topologies. In cascaded H-bridge converters, each submodule must be powered by its own isolated DC source, which complicates the power supply arrangement. In contrast, the half-bridge MMC shares a single common DC link across all submodules. This greatly simplifies the supply design and makes the MMC particularly attractive for medium- and high-voltage applications [35].

Figure 2 illustrates the structural difference between half-bridge and full-bridge SMs. The half-bridge offers reduced device count and higher efficiency but lacks inherent DC fault blocking capability. The full bridge provides fault blocking at the cost of additional components and higher losses. For the purposes of this work, the half-bridge MMC was selected, balancing simplicity, efficiency, and suitability for demonstrating the proposed balancing strategy.

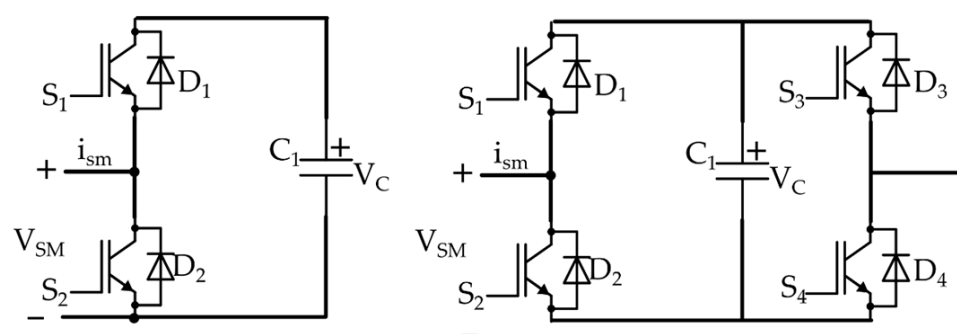


Figure 2. Half-bridge SM and full-bridge SM.

2.2. Mathematical Modelling of the MMC

The mathematical modelling of the modular multilevel converter (MMC) is fundamental for analysing and predicting its operational performance. Accurate models provide an insight into the complex behaviour and interactions between the various components of the MMC, thereby informing control design, stability analysis, and optimisation. Several modelling techniques have been proposed in the literature, including the phasor control model [35], switched-average model [36], and the equivalent circuit model [37]. Among these, the equivalent circuit model stands out due to its balance between feasibility, reliability, and computational efficiency.

In this work, a single-phase half-bridge MMC leg is considered as illustrated in Figure 3. Each arm is represented by the series connection of the inserted submodule capacitor voltages, an arm resistor, and an arm inductor. The midpoint between the upper and lower arms forms the AC terminal, while the converter is supplied by a common DC-link voltage V_{dc} .

For analytical simplicity, the upper and lower arms are assumed symmetric, i.e., $R_u = R_l$ and $L_u = L_l$ [36]. Furthermore, in this model, the external load resistance and inductance (R_o , L_o) are also set equal to these arm values for control-oriented simplification. This equivalence is a modelling simplification commonly adopted in control-oriented studies.

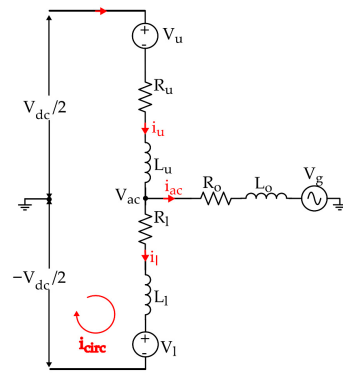


Figure 3. Single-phase MMC equivalent circuit.

The upper-arm current i_u is defined as positive downward, flowing from the positive DC bus to the AC node. The lower-arm current i_l is also defined as positive downward, flowing from the AC node to the negative DC bus. The AC current i_{ac} is defined as positive, flowing out of the converter into the grid, while the DC current i_{dc} flows from the DC source into the converter and is the sum of the upper and lower arm currents. With these definitions and based on Figure 3, the upper and lower arm currents (i_u and i_l) are therefore expressed as:

$$i_u = i_{circ} + \frac{1}{2}i_{ac} \quad (1)$$

$$i_l = i_{circ} - \frac{1}{2}i_{ac} \quad (2)$$

where i_{circ} and i_{ac} represent the internal circulating current and the AC output current, respectively. The circulating current and AC output current are then determined by:

$$i_{circ} = \frac{1}{2}(i_u + i_l) = \frac{1}{2}i_{dc} \quad (3)$$

$$i_{ac} = i_u - i_l \quad (4)$$

Applying Kirchhoff's Voltage Law (KVL) to the upper arm, along the path from the positive DC bus to the AC node, yields:

$$V_u = \frac{V_{dc}}{2} - L_u \frac{di_u}{dt} - R_u i_u - L_o \frac{di_{ac}}{dt} - R_o i_{ac} - V_g \quad (5)$$

Similarly, applying KVL to the lower arm, along the path from the AC node to the negative DC bus, yields:

$$V_l = \frac{V_{dc}}{2} - L_l \frac{di_l}{dt} - R_l i_l + L_o \frac{di_{ac}}{dt} + R_o i_{ac} + V_g \quad (6)$$

By subtracting the upper-arm voltage Equation (5) from the lower-arm voltage Equation (6), the expression for the AC node voltage V_{ac} is obtained as:

$$V_{ac} = \frac{1}{2} \left[(V_l - V_u) - R_o i_{ac} - L_o \frac{di_{ac}}{dt} \right] \quad (7)$$

Based on the equivalent circuit representation, the expression for the external grid voltage V_g at the point of common coupling (PCC) is given by:

$$V_g = V_{ac} - R_o i_{ac} - L_o \frac{di_{ac}}{dt} = \frac{1}{2} \left[(V_l - V_u) - 3(R_o i_{ac} + L_o \frac{di_{ac}}{dt}) \right] \quad (8)$$

Voltage balancing across submodule capacitors is fundamental to the MMC's safe and efficient operation. Any imbalance distorts the arm voltage synthesis, drives unequal power sharing, elevates harmonic distortion, and can precipitate instability. Therefore, the mathematical model must account for the dynamics of voltage balancing to ensure accurate performance prediction and reliable operation. The capacitor voltage ripple $\frac{dV_{ru}}{dt}$ and $\frac{dV_{rl}}{dt}$ play a significant role in maintaining balanced voltages across the submodules [37]:

$$\frac{dV_{ru}}{dt} = \frac{1}{NC} \left[i_{circ} + \frac{i_{ac}}{2} \right] \quad (9)$$

$$\frac{dV_{rl}}{dt} = \frac{1}{NC} \left[\frac{i_{ac}}{2} - i_{circ} \right] \quad (10)$$

The mathematical model assumes a single-phase equivalent circuit, which simplifies analysis while preserving the essential dynamics relevant for control design. This captures arm currents, terminal voltage, circulating current, and capacitor ripple behaviour, highlighting the importance of capacitor voltage balancing since any mismatch directly affects output voltage quality and stability. While conventional insertion-based methods [14] and nearest-level modulation [35] address this challenge, they suffer from scalability and computational overhead. To overcome these limitations, this work introduces a modified quick-sort-based balancing strategy, detailed in Section 2.3, which improves computational efficiency while maintaining real-time performance.

2.3. Control of Gate Driver/Switching Logic

As illustrated in Figure 3, the modular multilevel converter (MMC) requires accurately timed pulse signals to control the switching of its power devices. These pulses are typically generated using modulation techniques, with pulse width modulation (PWM) being one of the most widely employed approaches. PWM is particularly effective for regulating the AC output voltage of power converters as it minimises harmonic distortion and enhances the voltage gain at a given switching frequency. Over time, several PWM strategies have been developed for MMCs, which are broadly categorised into high-frequency and low-frequency modulation schemes [38]. Among these, the multicarrier PWM technique is widely adopted due to its straightforward integration of submodule capacitor voltage balancing. Multicarrier PWM can be further classified into two primary methods: phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM).

In the proposed MMC control scheme, level-shifted pulse width modulation (LS-PWM) is adopted due to its straightforward implementation and inherent compatibility with capacitor voltage balancing. As shown in Figure 4, LS-PWM employs two level-shifted carrier signals compared against a common sinusoidal reference, where their intersection points determine the submodule switching states, producing the desired three-level output voltage while promoting balanced capacitor utilisation.

In this paper, an open-loop modulation technique is adopted to generate the gate pulses sent to each power device, incorporating the proposed voltage balancing strategy. The reference voltages for the upper and lower arms are defined as:

$$V_u = \frac{V_{dc}}{2} - V_m \sin(\omega t) \quad (11)$$

$$V_l = \frac{V_{dc}}{2} + V_m \sin(\omega t) \quad (12)$$

where the amplitude voltage of the modulation signal V_m is given by:

$$V_m = M \cdot \frac{V_{dc}}{2} \quad (13)$$

with M denoting the modulation index. For a 3-level half bridge MMC, the upper and lower arms each require $N-1$ submodules, corresponding to the number of submodules per arm.

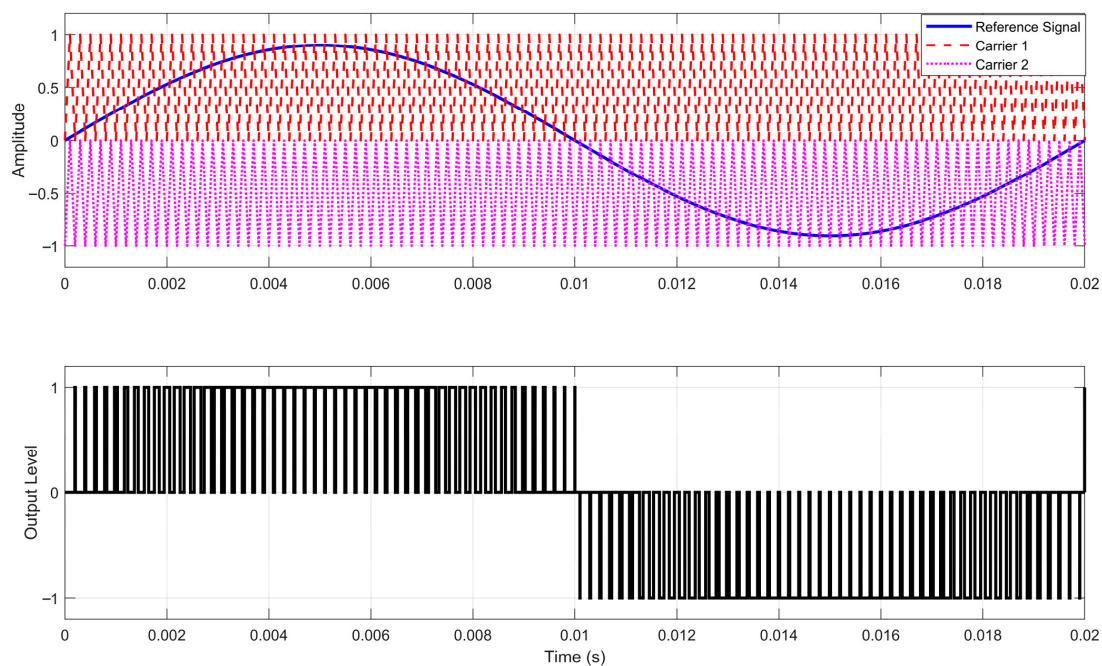


Figure 4. Reference and carrier signals using LS-PWM.

As shown in Figure 4, level-shifted PWM (LS-PWM) utilises multiple triangular carrier signals that are vertically shifted relative to one another. These carriers are simultaneously compared with the modulation signal to determine the switching states of the individual submodules. When the modulating signal exceeds a given carrier, the corresponding submodule is inserted; otherwise, it is bypassed. This approach enables the synthesis of a stepped multilevel output voltage while inherently distributing capacitor usage among submodules. The resulting modulation signals are fed into the enhanced voltage balancing algorithm, as illustrated in Figure 5.

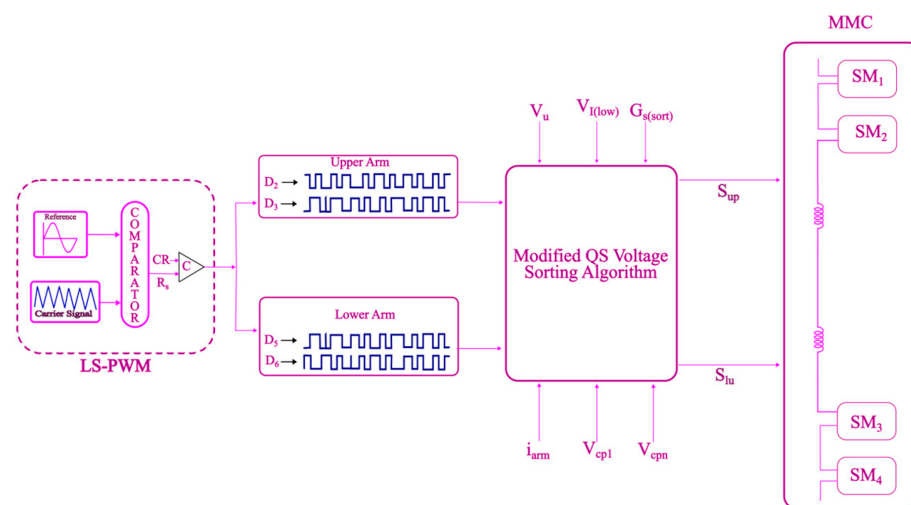


Figure 5. Primary control method for single-phase MMC.

In the MMC operating with LS-PWM, the comparison of reference and carrier signals determines submodule insertion. However, this modulation technique by itself does not

ensure capacitor charge/discharge balance, particularly in low-level MMC configurations (such as 3, 5, and 7 levels) where each submodule strongly influences output voltage and capacitor stability. To address this, a balancing mechanism is integrated with the modulation logic to guarantee long-term capacitor operation without additional circuits or feedback loops.

The proposed approach employs a modified quick-sort algorithm that ranks submodule capacitor voltages at each switching instant and uses the arm current direction as the decision variable for insertion. This combination ensures that power flow supports balancing: when current flows into the converter, the lowest-voltage submodule is prioritised for charging, while, when current flows out, the highest-voltage submodule is selected for discharging. The gate signal for submodule j is thus given by

$$S_j(t) = \begin{cases} 1, & j = i_{outL}(t), i_{arm}(t) > 0 \\ 1, & j = i_{outH}(t), i_{arm}(t) < 0 \\ 0, & otherwise \end{cases} \quad (14)$$

where

$S_j(t) \in \{0, 1\}$ is the gate signal of the submodule;

$i_{outL}(t)$ is the index of the submodule with the lowest capacitor voltage;

$i_{outH}(t)$ is the index of the submodule with lowest capacitor voltage;

$i_{arm}(t)$ is the instantaneous arm current.

A key modification introduced in this work is the use of dynamic pivot selection during sorting. At each switching period, the quick-sort algorithm selects a pivot element that divides the capacitor voltages into “lower” and “higher” subsets relative to the imbalance. The pivot is not fixed but chosen adaptively based on the instantaneous distribution of capacitor voltages. This allows the controller to target the most imbalanced submodule directly, rather than scanning or updating all indices exhaustively as in nearest-level or insertion-based methods. Another innovation is the incorporation of adaptive sorting depth, where the algorithm terminates early once the imbalance falls below a tolerance band. In practice, this means that only partial sorting is executed when capacitor voltages are already closely equalised. As a result, the average number of sorting operations per cycle is reduced, lowering computational burden while preserving balancing accuracy. This modification provides a quantifiable advantage over conventional full-depth sorting, which always processes all submodules regardless of imbalance.

The complete control sequence is illustrated in Figure 6a,b. Capacitor voltages are measured, sorted by magnitude, and perturbation is applied to resolve ties. The resulting indices are tracked, and the insertion logic is executed according to the arm current direction. At each switching cycle, only one submodule is selected for charging or discharging, which prevents overuse of individual SMs and ensures uniform degradation.

The algorithm was first implemented in MATLAB/Simulink, then exported as C code to Typhoon HIL. The typhoon HIL schematic is as shown in Figure 7 showing the power electronics section and exported C code. Preliminary debugging was performed in VHIL mode, while the final validation was carried out under PHIL conditions with the 3-level MMC prototype. For benchmarking, the proposed method is compared against conventional nearest-level and insertion-based algorithms, which do not employ dynamic pivot selection or adaptive sorting.

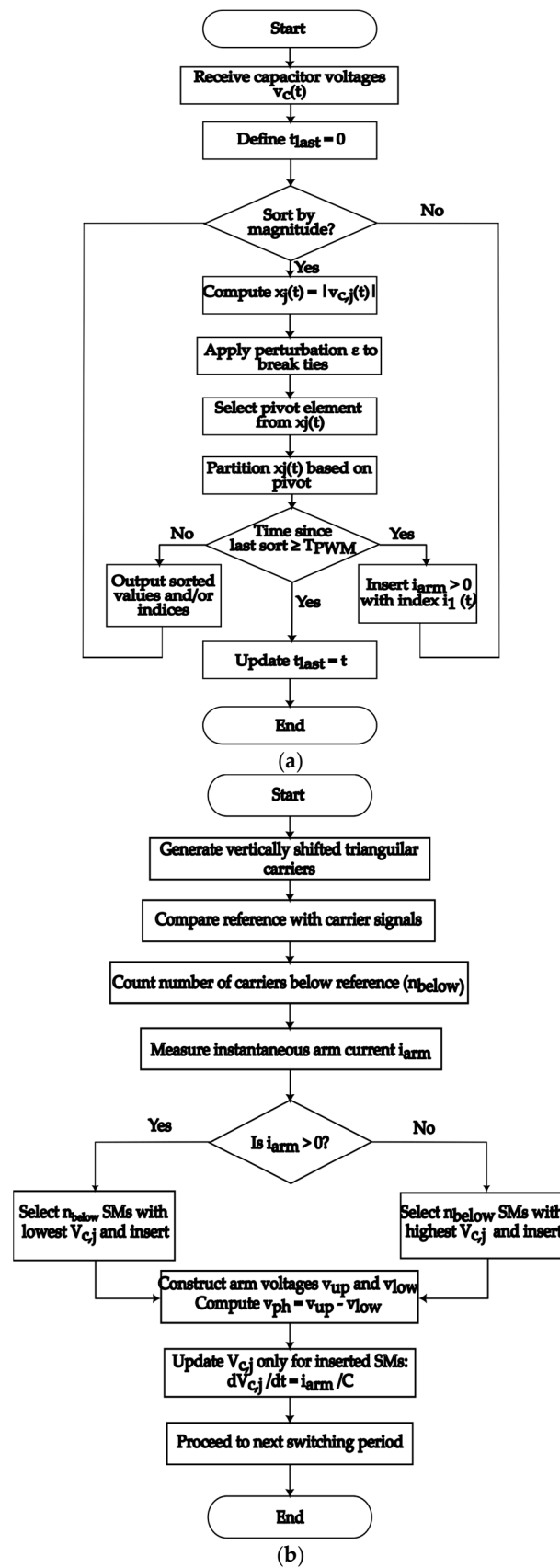


Figure 6. (a) Capacitor voltage-balancing scheme for MMC. (b) LS-PWM submodule switching insertion logic.

The proposed balancing procedure is summarised in Algorithm 1, which mirrors the control flow shown in Figure 6a. For clarity, this algorithm is expressed in abstract pseudocode form, highlighting the key steps of pivot selection, adaptive depth, and insertion logic.

Algorithm 1: Enhanced_Voltage_Balancing

```

1: Measure capacitor voltages  $V_j$ 
2: Determine number of SMs to be switched on
3: Select pivot dynamically based on  $V$  distribution and  $i_{arm}$ 
4: Partition  $V$  into two subsets:
    Lower set:  $V_j \leq V_{Pivot}$ 
    Higher set:  $V_j > V_{Pivot}$ 
5: Apply perturbation  $\varepsilon$  if two or more voltages are equal
6: Adaptive depth check:
    If  $\max(V) - \min(V) < \Delta\tau oI \rightarrow$  stop (terminate sorting early)
    Else  $\rightarrow$  continue sorting subsets recursively
7: Sort SMs and select index for insertion:
    If  $i_{arm} > 0 \rightarrow$  select SM with lowest  $V_j$ 
    If  $i_{arm} < 0 \rightarrow$  select SM with highest  $V_j$ 
8: Generate gate signal for selected SM
9: Update capacitor voltages for next cycle
end procedure

```

The sorting step has a complexity of $O(N \log N)$, while the adaptive depth termination reduces unnecessary recursive calls, yielding near-linear performance in practice. This makes the algorithm computationally efficient for real-time balancing.

In summary, the proposed modified quick-sort method integrates dynamic pivot selection and adaptive depth control with LS-PWM insertion logic. This combination reduces computational costs, scales effectively with increasing submodule number, and ensures reliable capacitor balancing under real-time constraints.

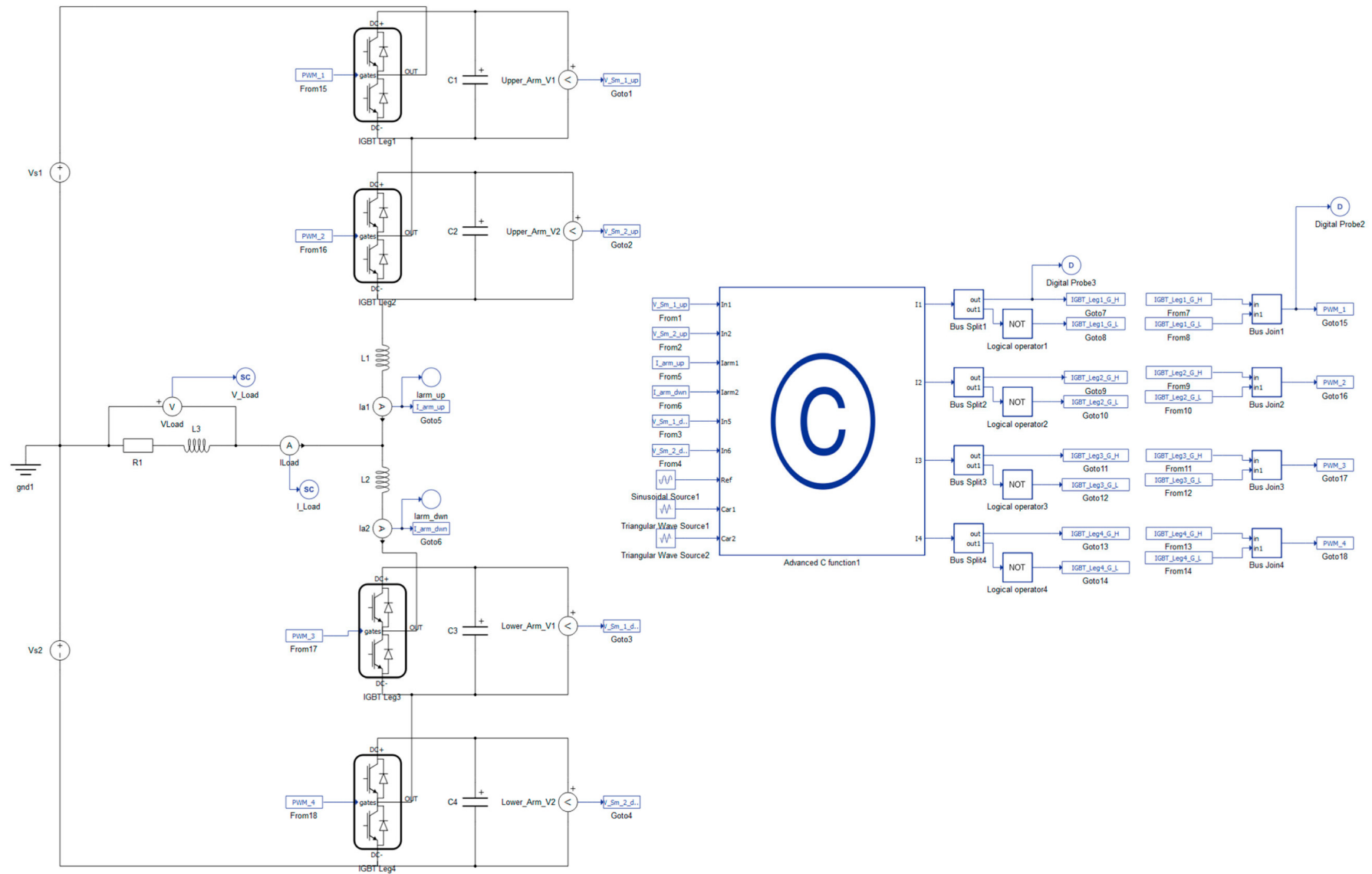


Figure 7. Typhoon HIL schematic showing 3-level half-bridge MMC and controller implemented in C.

2.4. Circuit Design and Prototype Development

The hardware design of the modular multilevel converter (MMC) was developed with a focus on modularity, scalability, and robustness to ensure reliable operation in power conversion applications. Figure 8 presents the block diagram of the designed half bridge MMC submodule, which is organised into three main building blocks: (a) power stage, (b) gate driver stage, and (c) measurement stage.

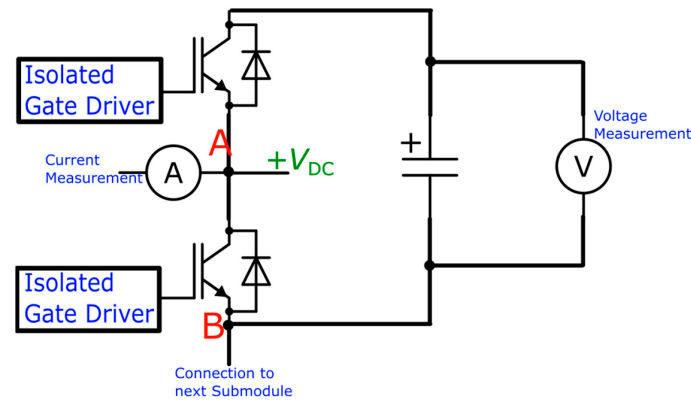


Figure 8. Half-bridge MMC submodule block diagram.

- (a) **Power Stage:** The power stage comprises the main switching devices (Insulated-Gate Bipolar Transistors, IGBTs) and onboard DC/DC converters that supply various voltage levels to the control and measurement circuits. The selected IGBT as listed in Table 1 support high switching frequencies and voltage levels suitable for MMC operation. Integrated protection circuits safeguard against overvoltage, overcurrent, and other fault conditions, enhancing system reliability.

Table 1. Hardware design components.

Equipment	Manufacturer	Model
Gate Driver	Infineon	1ED020I12-BT
Voltage Sensor	Broadcom (San Jose, CA, USA)	ACPL-C79B
Current Sensor	LEM (Meyrin, Switzerland)	LEM 25
IGBT	On Semi (Phoenix, AZ, USA)	FGH60N60SMD
Control Platform	Typhoon HIL	HIL 402

- (b) **Gate Driver Stage:** The gate driver circuitry, implemented using the Infineon 1ED020I12-BT (Infineon, Neubiberg, Germany) (listed in Table 1), provides galvanic isolation between the high-power and low-voltage control sections, ensuring noise immunity and operator safety. Hardware-based dead-time management is integrated within the driver to prevent shoot-through faults and enable fast transient response, improving overall switching reliability during high-frequency MMC operation.
- (c) **Measurement Stage:** Accurate monitoring of submodule voltages and arm currents is essential for balancing capacitor voltages and ensuring stable operation. The voltage-sensing circuit employs isolated differential amplifiers to accurately measure capacitor voltages while rejecting high common-mode voltages. A component-level protection method inspired by [39] was adapted to safely interface with high-voltage terminals of the IGBTs and capacitors.

A laboratory-scale MMC submodule was developed following a bottom-up approach, incorporating the design features. Figure 9 shows the developed half-bridge MMC sub-

module. The modular design enables scalable testing of various multilevel configurations and facilitates integration with the proposed capacitor balancing and LS-PWM modulation algorithms. The laboratory prototype uses 600 V, 60 A IGBTs (OnSemi FGH60N60SMD) driven by isolated gate drivers (Infineon 1ED020112-BT), giving the hardware a design capability in the tens of kilowatts based on device ratings. For PHIL validation, the operating point was deliberately kept in the sub-kilowatt range to ensure safe operation, manageable thermal conditions, and compatibility with the Typhoon HIL402 interface. Safety measures included fusing, galvanic isolation, emergency shut-off, and usage of current-limiting supplies.

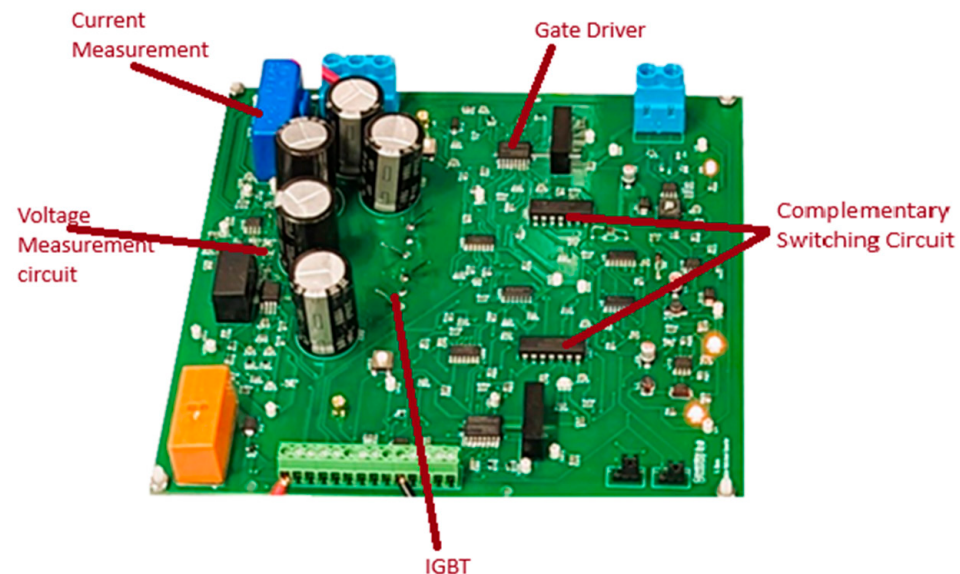


Figure 9. Designed half-bridge MMC prototype submodule.

3. Results and Discussion

The experimental evaluation of the control algorithm was carried out using a laboratory-scale three-level MMC prototype interfaced with the Typhoon HIL 402 platform. The control algorithm was first developed in MATLAB/Simulink and then exported to Typhoon HIL for algorithm validation. Typhoon HIL provides two modes: Virtual HIL (VHIL), which is simulation-only, and FPGA-based HIL running on the HIL402 hardware. While VHIL was initially used for debugging, the full implementation was validated using PHIL comprising the laboratory-developed prototype and the control algorithm running on Typhoon HIL. The I/O latency of the Typhoon HIL interface is negligible relative to the switching cycle and therefore does not affect the results.

The three-level MMC prototype was connected through a Texas Instruments (TI) Launchpad, which handled real-time communication between Typhoon HIL402 and the physical converter. This configuration enabled the controller to generate gate signals in real time, apply them to the prototype submodules, and receive measured voltages and currents back through the Launchpad interface. Figure 10 illustrates the overall setup, showing the development computer, Typhoon HIL402 with TI interface, the MMC prototype board, laboratory power supply, and RL load.

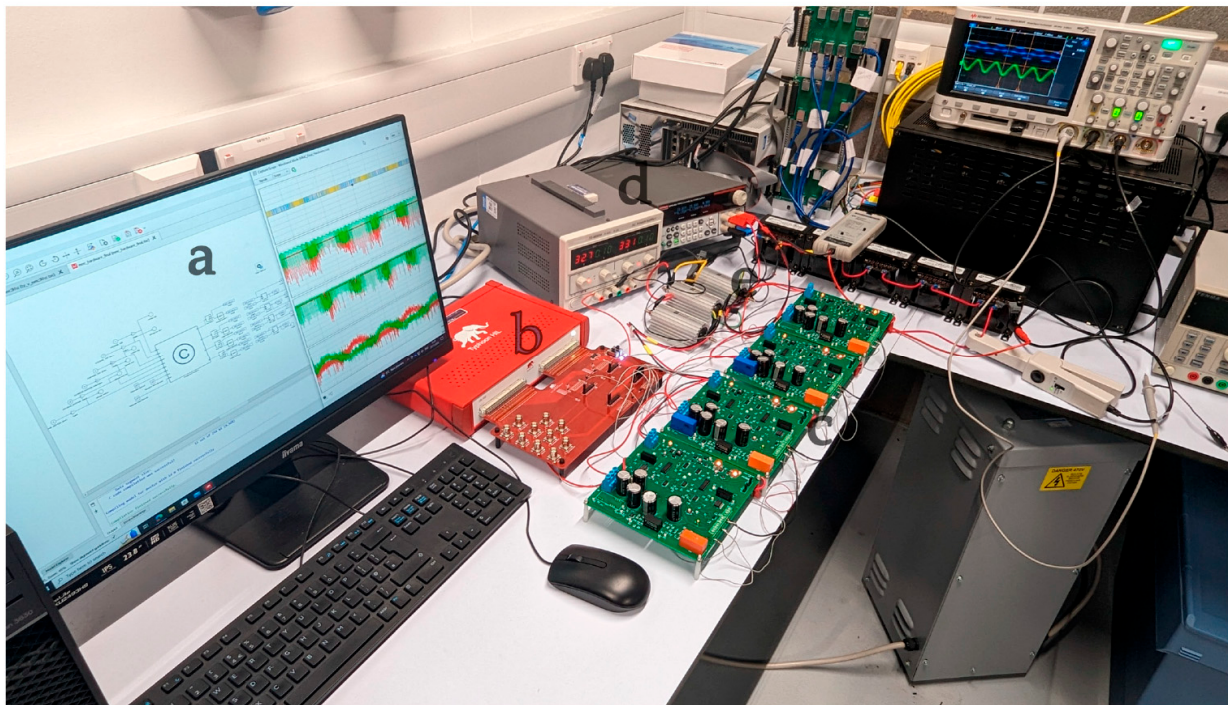


Figure 10. Experimental setup of built 3-level MMC. (a) Development computer. (b) Typhoon HIL + TI interface card. (c) Three-level MMC prototype. (d) Lab-based power supply. (e) RL load.

Through this PHIL arrangement, the proposed algorithm could be validated under realistic hardware conditions, capturing the effects of switching, capacitor dynamics, and load variations that are not present in pure simulations. MATLAB/Simulink was employed for controller design and automatic code generation, while additional tools such as Proteus (for PCB layout) and LTSpice (for component analysis) supported the hardware design workflow. HIL402 ensured that the balancing algorithm was tested under strict real-time constraints, thereby bridging the gap between offline modelling and physical prototyping.

Table 2 summarises the key experimental and simulation parameters used. The results obtained from this setup, presented in Figures 11 and 12, demonstrate the ability of the proposed control algorithm to maintain balanced capacitor voltages and synthesise a stable output AC waveform, even under dynamic load conditions.

Table 2. Experimental and simulation parameter setup values.

Parameter	Experimental Value
DC Source Voltage (V)	60
Number of Submodules/ Arm	2
Load Resistance (R1) (Ω)/Load Inductance (L3) (mH)	74/12.5
Arm Inductance (L1, L2) (nH)	2.5
Switching Frequency	3 kHz

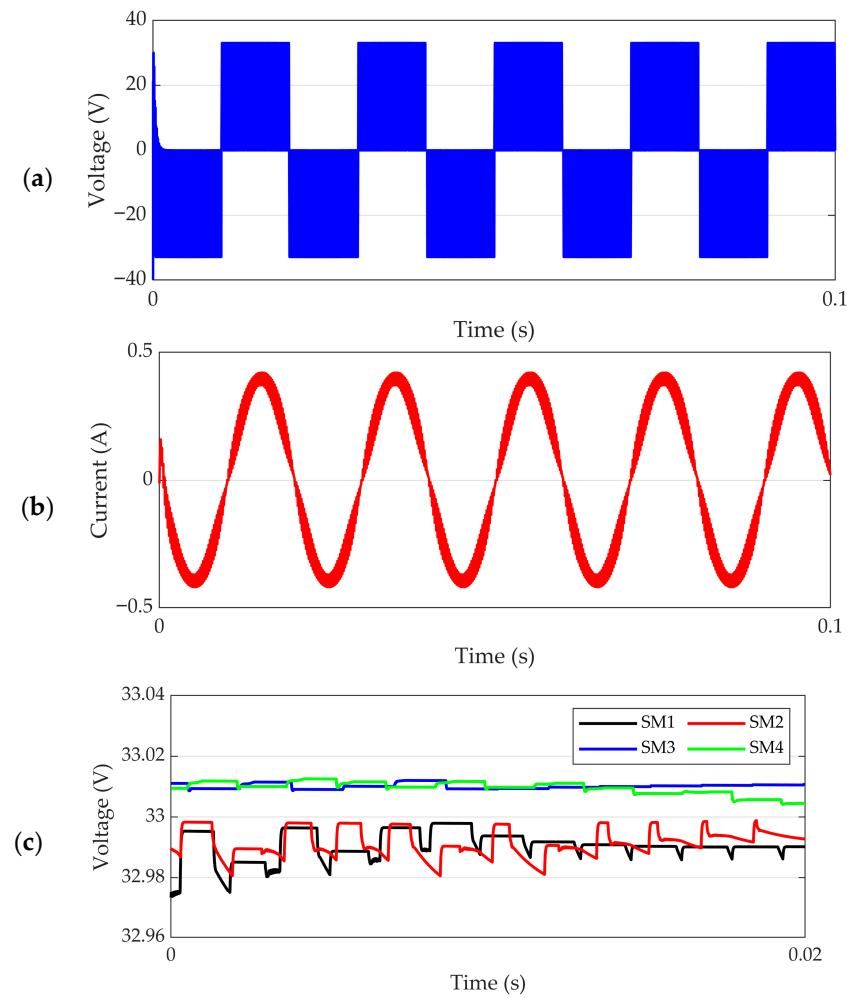


Figure 11. Simulink simulation results of modified 3-level MMC. (a) Output voltage, (b) capacitor voltages for upper and lower arms, and (c) output current.

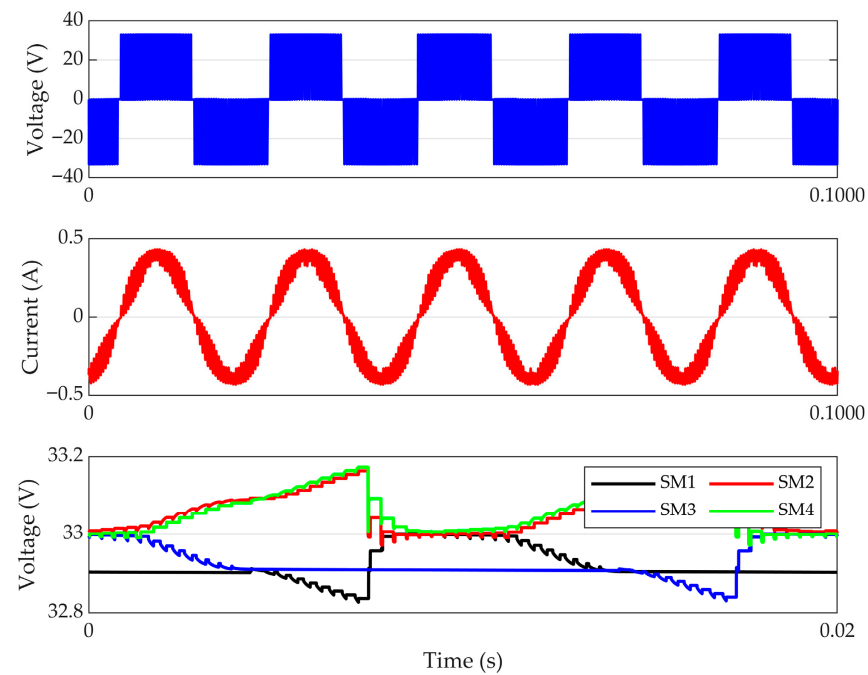


Figure 12. Typhoon Virtual HIL results showing output voltage, current, and capacitor voltages for all submodules.

The combined results from MATLAB/Simulink simulation, Typhoon Virtual HIL, and experimental hardware validation are presented in Figures 11–13. These show a consistent three-level stepped output voltage, confirming correct MMC operation across all platforms. The simulated waveforms are ideal and noise-free, and the hardware prototype maintains the expected three-level structure but with switching noise and measurement distortion due to practical parasitics. The current output remains sinusoidal in all cases, while the capacitor voltages are effectively balanced, with deviations remaining bounded despite increased ripple in hardware. This progression from clean simulation to noisier but stable hardware waveforms highlights both the robustness of the proposed balancing algorithm and the practical challenges of real implementation.

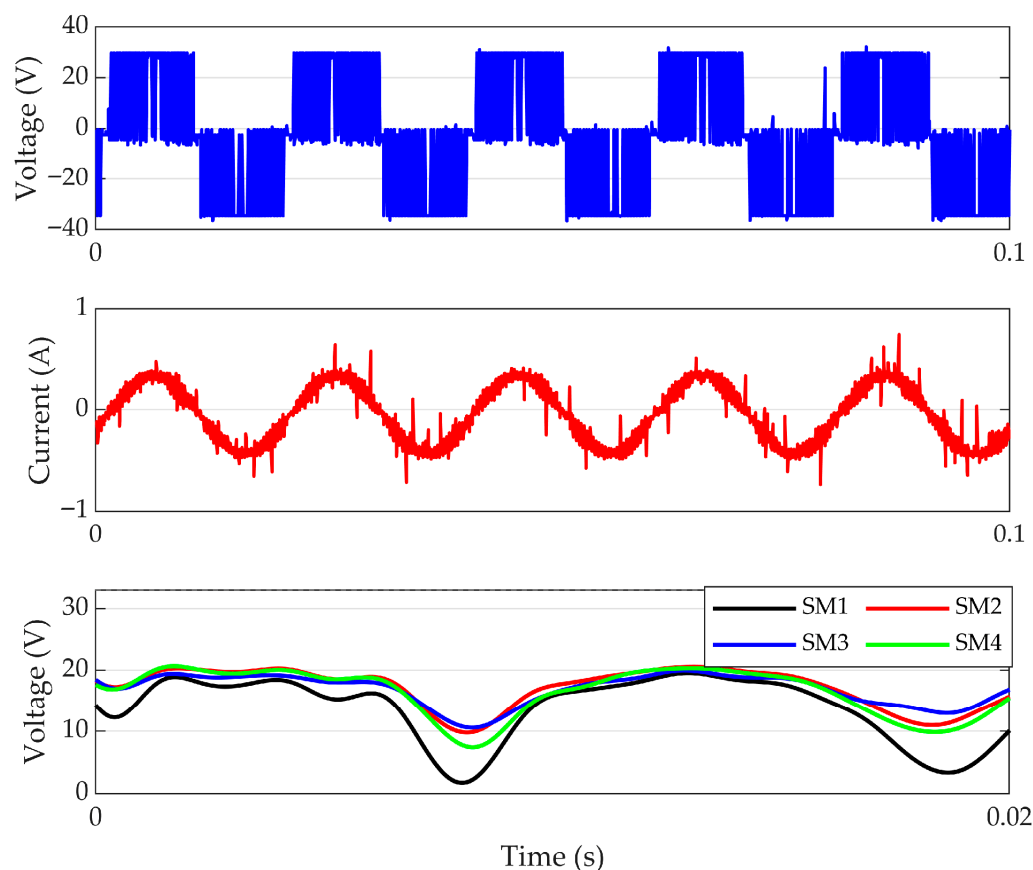


Figure 13. Experimental hardware results showing output voltage, current, and capacitor voltages for all submodules.

The proposed modified quick-sort method maintained capacitor voltages within $\pm 1\%$ deviation and limited THD to around 10%, while achieving $\sim 40\%$ faster execution compared to conventional sequential sorting. These results, consistent with the quantitative benchmarks in Table 3, demonstrate improved efficiency relative to PS-PWM (typically $\sim 15\%$ THD) and NLM (higher ripple, $\sim 10\text{--}15\%$), as reported in the recent literature [21–24]. By combining deterministic operation with adaptive depth and dynamic pivot selection, the method reduces redundant comparisons and scales more effectively with the number of submodules. Overall, the results validate that the algorithm is both computationally efficient and experimentally reliable, making it suitable for larger MMC systems and demanding applications such as high-voltage direct current (HVDC) transmission and renewable energy integration.

Table 3. Comparison of the proposed quick-sort balancing method with baseline approaches.

Metric	Baseline Methods (2020–2024)	Proposed Method	References
THD	Yu et al. [21]: PS-PWM ~15% THD in medium-scale MMCs; Gu et al. [23]: Hybrid MPC reduces harmonic distortion but adds control overhead.	~10%	[21–23]
Voltage Balancing Deviation	Abdayem et al. [22]: NLM ripple $\pm 10\text{--}15\%$; Lyu et al. [40]: Radix sorting reduced ripple but sensitive to fluctuations.	$\sim \pm 5\%$ peak-to-peak	[22,24,40]
Computational Efficiency	Sorting-based balance can become computationally heavy as submodule count grows	Significantly lower execution time (~40% faster) compared to native sorting	[24,40,41]

The computational analysis was performed using the Typhoon HIL compiler utilisation report, which evaluates execution time and memory constraints at compile time. This approach directly verifies that the proposed balancing algorithm satisfies real-time execution requirements, without the need for additional low-level software profiling. As shown in Table 3, the compiler reported 55% utilisation at a $1.0\ \mu\text{s}$ step, confirming feasibility with significant headroom.

Beyond the laboratory validation, these findings raise important considerations for scaling the algorithm to HVDC-class MMCs. Several practical hurdles must be addressed before real-world deployment. The first hurdle is communication latency across distributed submodule controllers. In a large MMC with hundreds of submodules per arm, message passing and coordination must be carefully managed to prevent delays from degrading balancing performance.

Second, component stress and thermal management become critical at HVDC ratings. Capacitor aging accelerates under higher voltage stress, and uneven thermal distribution can undermine long-term reliability. This requires both advanced cooling solutions and redundancy to maintain stable operation.

Third, fault management and redundancy must be considered. Large-scale MMCs are typically required to continue operating under submodule failures, which place additional demands on the balancing algorithm to reallocate switching without introducing instability.

Finally, system integration with grid protection and control layers introduces complexity. HVDC schemes demand strict compliance with protection protocols, and balancing algorithms must not interfere with higher-level control objectives such as DC fault ride-through, black start, or frequency support.

Addressing these hurdles will be essential for transitioning from laboratory validation to utility-scale deployment. Future research will therefore focus on assessing the scalability of the proposed algorithm under communication-constrained environments and on validating its performance when integrated with protection and fault-tolerant control strategies in HVDC applications.

4. Conclusions

This study has presented and validated a modified quick-sort algorithm for capacitor voltage balancing in a three-level modular multilevel converter (MMC). The main contribution lies in introducing a dynamic pivot selection and adaptive sorting depth mechanism, which sets the method apart from conventional balancing techniques that rely on fixed thresholds or exhaustive comparisons. By embedding this algorithm within a real-time hardware-in-the-loop (HIL) environment, this study demonstrates that the computational

growth with increasing submodule numbers is mitigated compared to conventional approaches. Although experimental validation on Typhoon HIL 402 was limited to four half-bridges per arm due to hardware constraints, the method exhibited lower computational burden than sequential techniques and remains a promising candidate for larger converters if tested on higher-capacity HIL or FPGA platforms.

The results showed that the method kept the capacitor voltage ripple within about $\pm 5\%$ under steady load conditions. This is a clear improvement compared with around $\pm 12\%$ ripple reported in earlier studies of conventional methods. These results demonstrate that the method is not only accurate but also faster, which is especially valuable when converters with many submodules need to be controlled in real time.

Typhoon HIL testing confirmed that the method works under realistic operating limits. The system allowed for the effect of the limited frequency range that the HIL can handle, as well as the small delay caused by the HIL interface, which was measured as less than two microseconds. The VHIL tests agreed closely with MATLAB/Simulink simulations, which supports the accuracy of the approach. The tests also revealed practical limits such as the maximum number of submodules that could be simulated, some noise in current measurements, and restrictions in the Texas Instruments interface card (permits only four analogue input signals). All of these were managed during the experiment.

For future use in high-voltage direct current (HVDC) systems, this study points out some challenges. These include the need to deal with communication delays across large systems, the stresses that high power places on components, and the need for back-up schemes in case of faults. This means that, for full-scale projects, balancing methods must be able to cope with delays and remain reliable under heavy operating conditions.

In this study, the proposed quick-sort-based balancing algorithm was compared mainly with traditional methods such as sequential sorting and nearest-level modulation, demonstrating superior computational efficiency and balancing performance. It is noted, however, that recent approaches including radix sorting, hybrid predictive control, and reinforcement-learning-based balancing have also been investigated in the literature. While a detailed comparison with these advanced methods lies beyond the present scope, they represent promising directions for future benchmarking and could serve as a basis to extend this work further.

Overall, the results validate that the algorithm is both computationally efficient and experimentally reliable, making it suitable for larger MMC systems and demanding applications such as high-voltage direct current (HVDC) transmission and renewable energy integration.

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Conflicts of Interest: Author Wissam Jamal was employed by the company Albacom Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Nomenclature

Symbol/Acronym	Description
Acronym	
MMC	Modular Multilevel Converter
HVDC	High-Voltage Direct Current
HIL	Hardware in the Loop
VHIL	Virtual Hardware in the Loop
PHIL	Power Hardware in the Loop
PS-PWM	Phase-shifted Pulse Width Modulation
LS-PWM	Level-shifted Pulse Width Modulation
NLC	Nearest Level control
THD	Total Harmonic Distortion
SM	Submodule
IGBT	Insulated Gate Bipolar Transistor
Symbols	
V _{dc}	DC-link voltage
i _{dc}	the per-leg DC current
i _{ac}	AC-side output current
i _{circ}	Circulating current within the MMC arms
V _g	AC-side output voltage
V _u , V _l	Upper and Lower Arm Voltage
i _u , i _l	Upper and Lower Arm Current
R _u , L _u	Upper arm resistance and Inductance
R _l , L _l	Lower arm resistance and Inductance
R _o , L _o	External Load Resistance and Inductance
N	Number of submodules
C	Capacitance of capacitor
S1, S2, S3, S4	IGBT switches in circuit diagrams
D1, D2, D3, D4	Anti-parallel diodes of IGBTs

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