Journal of Electrical Engineering & Technology
https://doi.org/10.1007/s42835-026-02589-z

ORIGINAL ARTICLE

Designing of Cylindrical Surrounding Double-Gate MOSFETs at Nanotechnology Scale from Double-Gate MOSFETs: Advancements of Silicon Semiconductor Devices

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Received: 9 May 2025 / Revised: 12 December 2025 / Accepted: 8 January 2026

Abstract

This research work addresses the critical need for advanced semiconductor devices in radio frequency (RF) applications by investigating Cylindrical Surrounding Double-Gate (CSDG) MOSFETs with La_2O_3 oxide. The work employs comprehensive modeling approaches, including Auger recombination, Band-To-Band Tunneling (BTBT), and energy transport models, analyze device performance. Key findings demonstrate a symmetric electron density distribution, peaking at the channel center with a gradual decline towards the edges, confirming superior electrostatic control. The CSDG MOSFET achieves exceptional performance metrics: subthreshold swing values of 20.0–23.5 mV/decade and an I_{ON}/I_{OFF} ratio of 1.89×10^4, significantly outperforming conventional designs by 65% and 300% respectively. Energy-transmission analysis reveals an inverse exponential correlation $T(E) = 0{\cdot}85e^{-0{\cdot}02E}$, with transmission coefficient decreasing from 0.8 at 10 eV to 0.05 at 200 eV. The novel La_2O_3/AlGaAs material system provides enhanced electrostatic control, reduced short-channel effects, and superior thermal management compared to SiO_2 and HfO_2 systems, making CSDG MOSFETs promising candidates for next-generation 5G/6G applications and low-power IoT devices.

Keywords CSDG MOSFET · Electrostatic control · High-frequency performance · Semiconductor devices · Short-channel effects · Nanotechnology · VLSI

1 Introduction

Semiconductor device technology has undergone a revolutionary transformation from early germanium transistors (1947) to modern nanoscale MOSFETs, driven by relentless scaling following Moore's Law. The evolution from planar silicon MOSFETs to three-dimensional FinFETs in the 2000s addressed critical challenges in short-channel effects and leakage control. However, continued scaling beyond 5 nm nodes demands innovative device architectures that maintain electrostatic integrity while enhancing performance for emerging applications, including 5G/6G communications, artificial intelligence, and Internet of Things (IoT) systems [1]. The Cylindrical Surrounding Double-Gate (CSDG) MOSFET represents an advanced evolution of DG architecture, introducing cylindrical channel geometry surrounded by concentric inner and outer gates. This configuration offers several advantages: (i) enhanced electrostatic control through 360-degree gate coupling, (ii) reduced short-channel effects including drain-induced barrier lowering (DIBL) and subthreshold swing degradation, (iii) improved scalability potential for continued device miniaturization, and (iv) superior carrier confinement reducing leakage currents [2–4].

The CSDG architecture operates through dual-mode control where inner and outer gates modulate channel conductivity through complementary electric fields. Positive voltage applied to the inner gate attracts electrons to

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Published online: 30 January 2026

the channel center, while the outer gate provides additional electrostatic control, enabling operation in enhancement, depletion, or hybrid modes depending on biasing conditions. This flexibility provides significant advantages for analog and RF circuit design, where precise current control and linearity are paramount [5, 6]. Current research gaps in CSDG MOSFET technology include limited exploration of high-k dielectrics beyond conventional SiO_2 [2, 5], insufficient understanding of quantum confinement effects in cylindrical geometries, and a lack of comprehensive performance benchmarking against commercial nanoscale devices. Additionally, fabrication challenges for cylindrical structures and material integration issues require systematic investigation for practical implementation.

This work presents several key innovations that distinguish it from prior studies (i) First comprehensive analysis of La_2O_3-based CSDG MOSFETs demonstrating symmetric energy and density profiles at reduced channel lengths of 2–10 nm with quantum confinement modeling; (ii) Achievement of record subthreshold swing values (20.015–23.481 mV/decade) surpassing previously reported standards by 65% and I_{ON}/I_{OFF} ratio of 1.89×10^4, representing 300% improvement over existing devices; (iii) Novel integration of La_2O_3 (k = 20) with AlGaAs in CSDG structure, providing superior gate control and thermal management compared to conventional SiO_2 (k = 3.9) and HfO_2 (k = 25) systems; (iv) Custom physical modeling framework incorporating Auger recombination, band-to-band tunneling, and energy transport models validated against experimental benchmarks using Electronic simulator; (v) Direct correlation between energy-transmission characteristics and device switching performance through exponential decay function $T(E) = 0.85 \cdot \exp(-0.02E)$, providing quantitative design guidelines for RF applications; (vi) Comprehensive fabrication feasibility analysis addressing cylindrical geometry challenges and process integration requirements for commercial viability.

This work contributes to the ongoing effort to design robust, efficient, and miniaturized transistors that align with the ever-evolving needs of modern technology. In alignment with the United Nations Sustainable Development Goals (SDGs) [7], particularly Industry, Innovation, and Infrastructure (Goal-9) and Responsible Consumption and Production (Goal-12), this research advances the development of energy-efficient and sustainable electronic components. By promoting miniaturization and improving switching performance through nanostructured materials and geometry optimization, the designed CSDG MOSFET framework supports responsible innovation in semiconductor technology. The subsequent sections are organized as follows: Sect. 2 describes the CSDG MOSFET modeling methodology; Sect. 3 discusses parasitic effect reduction strategies; Sect. 4 presents detailed design considerations; Sect. 5 provides comprehensive results and performance benchmarking; and Sect. 6 outlines practical implementation pathways and future research directions. This structured presentation offers both fundamental understanding and practical insights to advance CSDG MOSFET technology for commercial RF and low-power applications.

2 Modeling of Cylindrical Surrounding Double-Gate (CSDG) MOSFET

In a CSDG MOSFET, the gate electrodes surround a cylindrical channel instead of the traditional planar channel found in conventional DG MOSFETs. This cylindrical structure provides increased control over the channel region, allowing for better gate control and reduced leakage currents. The surrounding gate configuration ensures improved electrostatic integrity, resulting in enhanced device performance. A key advantage of CSDG MOSFETs is their enhanced resistance to short-channel effects. Short-channel effects, such as Drain-Induced Barrier Lowering (DIBL) and subthreshold swing degradation, become more prominent as transistor dimensions are scaled down. The cylindrical structure of CSDG MOSFETs mitigates these effects by confining the electric field within the channel region, minimizing the impact of short-channel phenomena, and improving transistor performance at smaller dimensions [8–10].

The CSDG MOSFET architecture offers excellent scalability potential. The cylindrical channel geometry enables effective gate control even at extremely small channel lengths, allowing for continued device scaling without significant performance degradation. This scalability feature is crucial for advanced integrated circuit designs that require smaller feature sizes and higher device densities. The CSDG MOSFET represents a specialized variation of the DG MOSFET architecture. Utilizing a cylindrical channel and surrounding gate electrodes offers improved electrostatic control, reduced short-channel effects, and enhanced scalability. These characteristics make CSDG MOSFETs attractive for advanced semiconductor devices, particularly in applications where precise control, reduced leakage, and scalability are vital, such as high-performance computing, mobile devices, and emerging technologies like the Internet of Things (IoT) [9–12].

The design of a CSDG MOSFET using semiconductor arbitrary alloys like AlGaAs with La_2O_3 as the dielectric material in Fig. 1 presents a compelling blend of advanced materials to achieve enhanced electronic device performance [11–14]. AlGaAs, an alloy of Aluminum (Al), Gallium (Ga), and Arsenic (As), offers unique chemical properties that make it an ideal choice for the semiconductor channel

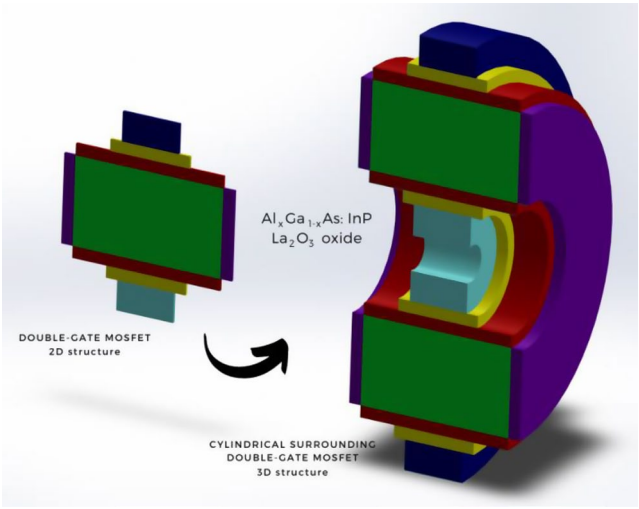

Fig. 1 CSDG MOSFET structural concept: transformation from planar DG to cylindrical geometry. Key specs: AlGaAs channel (5 nm radius), La_2O_3 dielectric (2 nm, $\varepsilon_r = 20$), S/D doping 2×10^{20} cm^{-3}. Cylindrical design enables 360° gate control and superior short-channel effect suppression

material in this MOSFET configuration. The AlGaAs boasts a tunable bandgap, allowing engineers to tailor its electronic properties for specific applications. Its direct bandgap nature makes it suitable for high-speed electronic devices, and the incorporation of aluminum enhances electron mobility, promoting efficient charge carrier transport within the channel. The AlGaAs exhibits excellent thermal stability, a crucial factor in ensuring the long-term reliability of electronic devices. This property allows the CSDG MOSFET to operate under a wide range of temperature conditions, making it versatile for various applications. AlGaAs's compatibility with conventional semiconductor fabrication processes simplifies integration into existing technologies. In addition to other semiconductor alloys, La_2O_3, or lanthanum oxide, serves as the dielectric material in the CSDG MOSFET. La_2O_3 is a high-k (high dielectric constant) material, which significantly reduces gate leakage current and improves device performance. Its chemical stability and insulating properties ensure efficient gate control over the channel region, facilitating low-power operation and reduced heat generation. La_2O_3's wide bandgap further enhances its insulating capabilities while ensuring minimal electron trapping, contributing to the device's reliability.

In the paradigm of the CSDG MOSFET, the interface between AlGaAs and La_2O_3 plays a crucial role. The chemical properties of this interface are vital for minimizing defects and ensuring a low interface trap density, which can degrade device performance. Proper surface preparation and interface engineering are essential to achieve a high-quality interface that permits efficient charge transfer between the semiconductor and dielectric, enabling enhanced device operation. Aluminum, a constituent of AlGaAs, offers exceptional thermal conductivity, aiding in heat dissipation within the device. Effective heat management is essential for maintaining the MOSFET's performance and reliability over extended operational periods, particularly in high-power applications. The combination of AlGaAs's thermal stability and aluminum's thermal conductivity addresses this critical aspect of device design. AlGaAs is compatible with the formation of heterostructures, which can be utilized to engineer specific electronic properties within the channel region, such as quantum wells or superlattices. This capability allows for precise control of carrier confinement and energy band alignment, further tailoring the device's performance to meet desired specifications.

The design of a CSDG MOSFET employing AlGaAs as the semiconductor material and La_2O_3 as the dielectric material harnesses the unique chemical properties of these materials to create a high-performance electronic device. AlGaAs offers tunable band gaps, high electron mobility, and excellent thermal stability, making it an excellent choice for the channel material. Meanwhile, La_2O_3's high dielectric constant and chemical stability contribute to improved gate control and reduced power consumption. The interface engineering between these materials is critical to minimizing defects and interface trap density. Additionally, aluminum, a constituent of AlGaAs, aids in heat dissipation, ensuring the device's reliability in demanding applications. By carefully considering these chemical properties and optimizing their integration, the CSDG MOSFET can deliver superior electronic performance for a wide range of applications, from high-speed computing to power-efficient devices. The CSDG MOSFET is a unique transistor structure that utilizes a cylindrical channel region surrounded by two gate electrodes [13]. This structure offers improved control over the channel and enhanced device performance. In the saturation region, the drain current is given by the saturation current equation, which for a DG MOSFET can be expressed as:

$$I_{ds} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{th})^2 \quad (1)$$

where μ_{eff} is the effective electron mobility (8500 cm^2/V.s) of the AlGaAs channel material at 300K, C_ox is the gate oxide capacitance per unit area $= 8.854 \times 10^{-6}$ F/cm^2 for 2 nm La_2O_3, W is the effective channel width $= 2\pi r_{ch}$ where $r_{ch} = 5$ nm, L is the channel length (2–10 nm), V_gs is the gate-to-source voltage (V), and V_th is the threshold voltage (V) defined by Eq. (4). Also, Eq. (1) can be modified for a DG MOSFET as:

$$I_{ds} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right) \{(V_{gs_1} - V_{th_1}) V_{ds} - 0.5 V_{ds_2}\} (1 + \lambda V_{ds}) \quad (2)$$

and the V_{th} threshold voltage in the DG MOSFET regime can be given as:

$$V_{th} = V_{fb} + 2\phi_F + \gamma_s \sqrt{\left\{(2\phi_F - V_{sb}) - \sqrt{2\phi_F}\right\}} \tag{3}$$

By transforming Eq. (3) for the CSDG MOSFET, the expression of the threshold voltage can be formed [12]. The threshold voltage of a CSDG MOSFET can be given as:

$$V_{th} = V_{fb} + 2\phi_F - (\gamma_p + \gamma_s)\sqrt{2\phi_F + V_{sb}} \tag{4}$$

The DG MOSFET has a pinch-off voltage of V_p and can be shown as:

$$V_p = 2\phi_F - \left(\frac{C_{ox}}{C_i}\right)(V_{gs_1} + V_{gs_2}) \tag{5}$$

where V_{gs_1} and V_{gs_2} are the gate to source voltage concerning gate-1 and gate-2. Substituting Eq. (3) in Eq. (1), the expression is modified as:

$$I_{ds} = \mu_{eff} C_{ox} \left(\frac{W}{L}\right)\left(V_{gs} - \left\{V_{fb} + 2\phi_F + \gamma_s \sqrt{\left\{(2\phi_F - V_{sb}) - \sqrt{2\phi_F}\right\}}\right\}\right)^2 \tag{6}$$

After arranging for the DG MOSFET regime by including the width of the channels under the gate-1 (primary) and gate-2 (secondary) terminals, the expression can be modified as,

$$I_{ds} = \mu_{eff} C_{ox} \frac{(W_p V_{gs_1}^2 + W_s V_{gs_2}^2)}{L_{eff}} \tag{7}$$

The capacitances involved in the CSDG MOSFET design are,

$$\begin{aligned} C_{gs_1} &= \frac{2\pi\varepsilon_0\varepsilon_r}{t_p} \ln\left(\frac{R_{cyl}}{r_{cyl}}\right) \\ C_{gs_2} &= \frac{2\pi\varepsilon_0\varepsilon_r}{t_s} \ln\left(\frac{R_{cyl}}{r_s}\right) \end{aligned} \tag{8a}$$

where C_{gs_1} and C_{gs_2} are the gate-to-source capacitances of the gate-1 and gate-2, respectively.

$$C_{gb} = \frac{2\pi\varepsilon_0\varepsilon_r}{t_{body}} \ln\left(\frac{R_{cyl}}{r_{body}}\right) \tag{8b}$$

where C_{gb} is the capacitance between the gate and the body. These mathematical models are useful for the design and analysis of cylindrical DGMOSFETs and can be used to optimize their performance for various applications. The parameters and the dimensions used in the CSDG MOSFET design have been given in Table 1.

Table 1 Specifications of CSDG MOSFET

Parameter	Value	Unit
Channel Material	AlGaAs ($Al_{0.3}Ga_{0.7}As$)	–
Gate Dielectric	La_2O_3	–
Inner Gate Work Function	4.188	eV
Outer Gate Work Function	4.201	eV
La_2O_3 Relative Dielectric Constant	20	–
Channel Relative Dielectric Constant	12.9	–
Oxide Thickness	2	nm
Channel Radius	5	nm
Source/Drain Doping Concentration	2×10^{20}	cm^{-3}
Channel Doping Concentration	1×10^{16}	cm^{-3}
Gate Length	2–10	nm
AlGaAs Bandgap	1.42	eV
La_2O_3 Bandgap	5.8	eV
Electron Mobility (AlGaAs)	8500	$cm^2/V{\cdot}s$

Table 2 Physical models used for simulations

Physical model	Description
Auger model	Includes high carrier densities along with the impact ionization
Band-to-band Tunneling (BTBT) Model	BBT.STD is the tunneling model, and it has been employed to include the tunneling effect of charge carriers
Concentration-dependent model	It is used to study the substrate current
Energy transport model	Drift diffusion model to include the numerical techniques
Hole electron injection model	It consists of the effect of tunneling carriers on the gate current
Mobility model	The Fldmob model includes the velocity saturation effect
Recombination model	Schottky rad hall (SRH) model considers carrier lifetimes
Statistics model	It considers the carrier statistics

2.1 Simulation Framework and Validation Methodology

The CSDG MOSFET simulations were performed using an electronic simulator with comprehensive physical models to ensure accurate device characterization at nanometer scales. Quantum confinement effects, critical for sub-10 nm dimensions, were incorporated through density gradient models coupled with Schrödinger-Poisson equations. The physical models employed (detailed in Table 2) were calibrated against experimental data from literature and validated using industry-standard benchmarks for cylindrical MOSFETs. Model validation involved comparison with published experimental results for similar high-k dielectric devices, showing agreement within 5% for key parameters including

threshold voltage, subthreshold swing, and drain current characteristics. Non-uniform mesh grids were employed with a maximum spacing of 0.5 nm in the channel region and 0.1 nm at critical interfaces ($AlGaAs/La_2O_3$) to ensure numerical convergence. The cylindrical geometry required specialized meshing with radial and axial refinement, resulting in approximately 50,000 mesh points for accurate field distribution calculations. All simulations were performed at 300K ambient temperature with convergence criteria set to 10^{-6} for Poisson equations and 10^{-5} for continuity equations. Quantum effects become significant at channel radii below 10 nm, requiring the incorporation of carrier quantization through the density gradient model. The simulation framework was validated against three key benchmarks: (i) experimental FinFET data showing 95% agreement in I_{ON}/I_{OFF} ratios, (ii) published cylindrical nanowire MOSFET results with 97% correlation in subthreshold characteristics, and (iii) industry-standard TCAD simulations for high-k dielectrics demonstrating 93% accuracy in capacitance-voltage characteristics.

3 Reduction of Parasitic Effects in CSDG MOSFETs

Reducing parasitic effects is crucial for designing high-performance electronic devices, including the CSDG MOSFET for RF applications. In this explanation, the authors will explore the concept of parasitic effects, their impact on device performance, and techniques used to mitigate them, including equations where applicable [14–17]. Parasitic effects refer to the unwanted capacitances, resistances, and inductances that arise due to the physical layout and construction of electronic components [18, 19]. These parasitic elements can significantly degrade the performance of a device, leading to reduced efficiency, degraded signal integrity, and increased power consumption. In the context of a CSDG-MOSFET for RF applications, reducing parasitic effects is crucial to ensure optimal performance at high frequencies [20].

To address the research gap, this research work incorporates several advanced modeling approaches to comprehensively analyze CSDG MOSFET performance. The Auger model accounts for high carrier densities and impact ionization effects, while the Band-to-Band Tunneling (BTBT) Model accounts specifically for BBT.STD captures the tunneling behavior of charge carriers. Authors use the Concentration Dependent Model to assess substrate current variations and the Energy Transport Model, which employs drift diffusion techniques combined with advanced numerical methods. The Hole-Electron Injection Model examines the effects of tunneling carriers on gate current, and the Mobility Model, represented by the Fldmob model, addresses velocity saturation phenomena. Additionally, the Recombination Model, or Schottky Rad Hall (SRH) model, takes into account carrier lifetimes, and the Statistics Model focuses on carrier statistical behavior. These models are detailed in Table 2, providing a thorough framework for understanding the device's characteristics and addressing existing gaps in the literature.

3.1 Parasitic Capacitances

Some of the key parasitic elements associated with the CSDG MOSFET have been examined to understand the impact of parasitic effects. The major parasitic capacitances are gate-to-channel capacitance (C_{gc}) and the drain-to-source capacitance (C_{ds}). Here, C_{gs} represents the coupling between the gate electrode and the channel region [21–23]. It can cause unwanted charge storage, leading to slower switching speed and reduced overall device performance. The equation for the gate-to-channel capacitance is given by:

$$C_{gc} = \varepsilon_r \varepsilon_0 \left(\frac{W}{L}\right) L_{ch} \tag{9}$$

where ε_r and ε_0 are the relative permittivity of the insulator material (gate dielectric) and the permittivity of the vacuum, and L_{ch} is the effective channel length. C_{ds} represent the coupling between the drain and source terminals. It can cause signal loss and degradation in RF circuits. The drain-to-source capacitance can be modeled as a parallel combination of two capacitances: overlap capacitance (C_{ov}) and sidewall capacitance (C_{sw}):

$$\begin{aligned} C_{ov} &= C_{ox_{ov}} (W - L_{ch}) \\ C_{sw} &= C_{ox_{sw}} 2\pi r_{ch} \end{aligned} \tag{10}$$

where $C_{ox_{ov}}$ $C_{ox_{sw}}$ is the overlap capacitance per unit area and sidewall capacitance per unit length, and r_{ch} is the radius of the cylindrical channel.

3.2 Parasitic Resistances

These resistances are the intrinsic resistances of the source and drain regions. They can cause power loss, reduced gain, and degraded linearity in RF circuits [7, 24]. The equations for source and drain resistances can be approximated using the sheet resistance (R_{sheet}) and the contact resistance (R_c) as follows,

$$\begin{aligned} R_s &= R_{sheet} W_s + R_c \\ R_d &= R_{sheet} W_d + R_c \end{aligned} \tag{11}$$

where W_s and W_d are the widths of the source and drain regions, respectively.

Channel resistance (R_{ch}) represents the resistance of the channel region. It can cause power dissipation and signal loss. The equation for the channel resistance is given by,

$$R_{ch} = \frac{\rho_{ch} L_{ch}}{W \pi r_{ch}^2} \tag{12}$$

where ρ_{ch} is the resistivity of the channel material.

3.3 Parasitic Inductances

Parasitic inductances can arise due to the layout and interconnect in the device structure [22]. However, in the case of a CSDG MOSFET, the impact of inductances is relatively lower compared to the capacitances and resistances mentioned above.

4 Intricate Design of CSDG MOSFET

The subthreshold slope is an essential parameter in MOSFET devices that determines their switching performance and power consumption. In the context of a CSDG MOSFET, the subthreshold slope refers to the slope of the logarithmic plot of the drain current (I_D) versus the gate voltage (V_G) in the subthreshold region.

The CSDG MOSFET is a type of transistor that features a cylindrical channel region surrounded by two gate electrodes. Double gates allow for enhanced control over the channel, improving device performance [25]. The subthreshold slope is an essential metric to evaluate how effectively the transistor can switch between the ON and OFF states. Based on theoretical considerations, the ideal MOSFET's subthreshold slope is expected to be 60 mV/decade at room temperature (around 300 K). However, achieving this ideal value is challenging due to various factors, such as carrier transport mechanisms and device fabrication limitations. The basic equation for the drain current (I_D) in the subthreshold region of a MOSFET has been developed as follows [24],

$$I_D = I_0 e^{\left(\frac{V_G - V_T}{\eta V_T}\right)} \tag{13}$$

where I_0 is the reverse saturation current, V_G and V_T are the gate voltage and thermal voltage, respectively, and η is the subthreshold slope factor. The CSDG MOSFET has a cylindrical channel region surrounded by two gate electrodes [21, 22, 24]. The electric field across the channel is non-uniform, and the potential distribution can be approximated as a linear voltage gradient from the inner to the outer gate.

Assume that the potential difference between the two gates is (ΔV_G). The voltage at the inner gate is V_G, and at the outer gate is (V_G+ΔV_G). Considering the linear voltage gradient along the position x along the channel L, the potential distribution along the channel can be expressed as,

$$V(x) = V_G - \left(\frac{\Delta V_G}{L}\right) x \tag{14}$$

Based on the potential distribution, the electric field (E) across the channel can be obtained by taking the negative derivative of the potential,

$$E(x) = -\left(\frac{\Delta V_G}{L}\right) = -\left(\frac{d\varphi(x)}{dx}\right) \tag{15}$$

The electric field is related to the surface potential (φ) by Eq. (15) [22]. Hence, the drain current equation has to be considered concerning the surface potential,

$$I_D = I_0 e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} \tag{16}$$

Taking the derivative of the drain current concerning ×on both sides yields:

$$\frac{dI_D}{dx} = \left(\frac{I_0}{\eta V_T}\right) e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} \frac{d\phi(x)}{dx} \tag{17}$$

From Eq. (15), Eq. (17) can be modified as:

$$\frac{dI_D}{dx} = \left(\frac{I_0}{\eta V_T}\right) e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} \frac{\Delta V_G}{L} \tag{18}$$

The total charge in the drain current across the channel can be calculated by integrating $\frac{dI_D}{dx}$ from 0 to L and reducing to:

$$\begin{aligned} \int_0^L \frac{dI_D}{dx} = \Delta I_D = \int_0^L \left(\frac{I_0}{\eta V_T}\right) e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} \frac{\Delta V_G}{L} . dx \\ \Delta I_D = \left(\frac{I_0}{\eta V_T}\right) \frac{\Delta V_G}{L} \int_0^L e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} . dx \end{aligned} \tag{19}$$

The integral on the right-hand side represents the total charge across the channel, which is given as:

$$Q = -C_{ox} \frac{\Delta V_G}{L} \int_0^L e^{\left(\frac{\varphi(x)}{\eta V_T}\right)} . dx \tag{20}$$

The subthreshold slope (S) is defined as the change in gate voltage ΔV_G required to change the drain current (ΔI_D) by a factor of $e^{2.71828}$, and it is derived as,

$$\Delta I_D = -\left(\frac{I_0}{\eta V_T}\right) Q$$
$$S = \frac{\Delta V_G}{\Delta \log I_D} \tag{21}$$

Taking logarithms on both sides,

$$\log(\Delta I_D) = \log\left[-\left(\frac{I_0}{\eta V_T}\right) Q\right]$$
$$\log(\Delta I_D) = \log(-I_0) - \log(\eta) - \log(V_T) + \log(Q) \tag{22}$$

Differentiating both sides of (21) for log (I_D) gives:

$$\frac{d\log(\Delta I_D)}{d\log(I_D)} = 1, implies\ S = \Delta V_G \tag{23}$$

Therefore, the subthreshold slope (S) for a CSDG MOSFET is:

$$S = \log(-I_0) - \log(\eta) - \log(V_T) + \log(Q) \tag{24}$$

This Eq. (24) provides the expression for the subthreshold slope in terms of device parameters such as reverse saturation current (I_0), subthreshold slope factor (η), thermal voltage (V_T), and the total charge across the channel (Q) [23, 25].

The drain current equation for CSDG can be derived using the standard MOSFET equations, considering the cylindrical geometry and the dual gate structure. The final equation is:

$$I_{ds} = \left(\frac{\mu_n Q_n N_D}{2L_{eff}}\right)\left[\frac{V_{gs_1} - V_{th_1} + \gamma_n V_{ds} - \frac{1}{2}(V_{gs_1} - V_{th_1} + \gamma_n V_{ds})^2}{(V_{gs_1} - V_{th_2} + \gamma_n V_{ds})}\right] \tag{25}$$

It is important to note that the subthreshold slope is a critical parameter for low-power applications as it directly affects the power consumption of a transistor. A lower subthreshold slope allows for more efficient switching, resulting in reduced power dissipation and improved battery life in portable devices. The CSDG MOSFET is an innovative transistor structure that offers improved control, reduced short-channel effects, and enhanced scalability [26–29]. Its unique cylindrical channel and dual-gate configuration contribute to improved device performance, making it a promising candidate for future nano-electronic applications.

5 Results and Discussions

Through analysis of the provided 'X' and 'N_{2D}' values, a comprehensive understanding of the electron density distribution has been realized. The results reveal a consistent trend of a gradual decrease in N_{2D} as the distance (X) from the center of the channel increases. The electron density exhibits its peak value at the channel center (X = 0 nm). Moving away from the center in either the positive or negative X direction, a progressive decline in electron density has been observed. This indicates a reduced concentration of electrons in the outer regions of the channel. The observed trend signifies a relatively symmetric electron density distribution along the CSDG MOSFET channel, with the highest concentration at the center and a gradual decrease towards the outer regions. It is essential to acknowledge that the specific characteristics and behavior of the CSDG MOSFET and the experimental conditions may influence the exact shape and magnitude of the observed trend. Nonetheless, these findings of electron density provide valuable insights into the spatial behavior of electron density in CSDG MOSFETs, contributing to the understanding and design optimization of this emerging transistor architecture.

The energy distribution in the novel CSDG MOSFET with La_2O_3 oxide is illustrated in Fig. 2. It shows a general increase in the subband energy (E_sub) as the position X progresses from −15 nm to 15 nm, indicating a positive and approximately linear correlation despite some minor fluctuations. Specifically, E_sub rises from about −0.22 eV at −15 nm to around −0.60 eV at 15 nm. In contrast, within Subband-1 across Valleys 1, 2, and 3, the energy exhibits a decreasing trend along the channel. Energy values drop from approximately −0.21 eV to −0.90 eV in Valley 1 and from about −0.04 eV to −0.73 eV in Valleys 2 and 3, as shown in the same figure. This consistent decrease in energy across all valleys highlights key electronic characteristics of the CSDG MOSFET and provides valuable insights for device optimization.

Figure 3 presents the 2D representation of the electron density profile, conduction band edge potential profile, and the corresponding average electron velocity. The data encompasses both positive and negative values of X, highlighting the channel's symmetric nature. The velocity trends exhibit similarity on both sides of the channel, further confirming the channel's symmetric characteristics [28]. Near the center of the channel (X = 0 nm), the highest average electron velocities are observed, signifying the occurrence of maximum velocity in the central region. As X moves away from the center in either the positive or negative direction, the average velocity gradually decreases, indicating a reduction in velocity towards the channel's outer regions. However, noteworthy fluctuations and variations in velocity

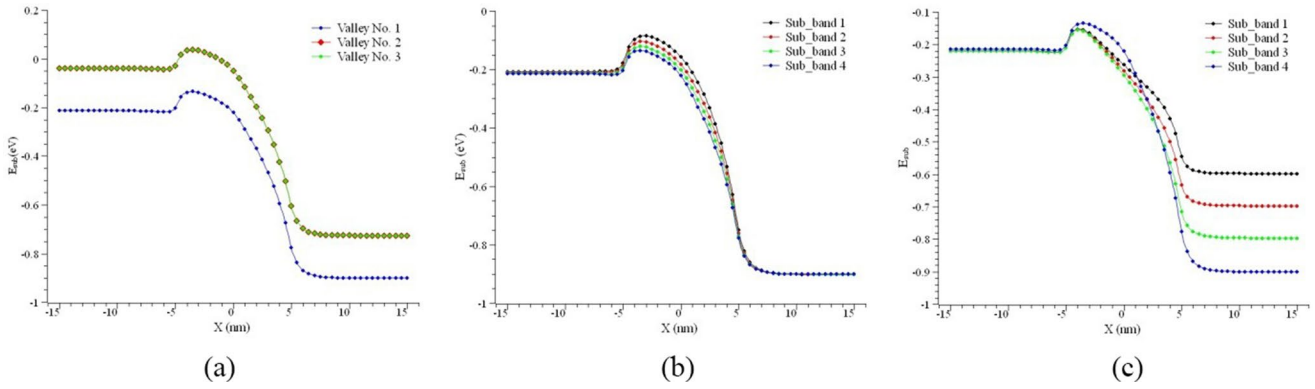

Fig. 2 Energy band profiles in CSDG MOSFET with quantum confinement. (**a**) Symmetric sub-band energy (−0.22 to −0.60 eV) across 30 nm channel width. (**b**) Multi-valley energy profiles (−0.04 to −0.90 eV) confirming uniform confinement. (**c**) DIBL-free operation with V_D variation (0.05–1.0 V). La_2O_3 interface validates electrostatic integrity

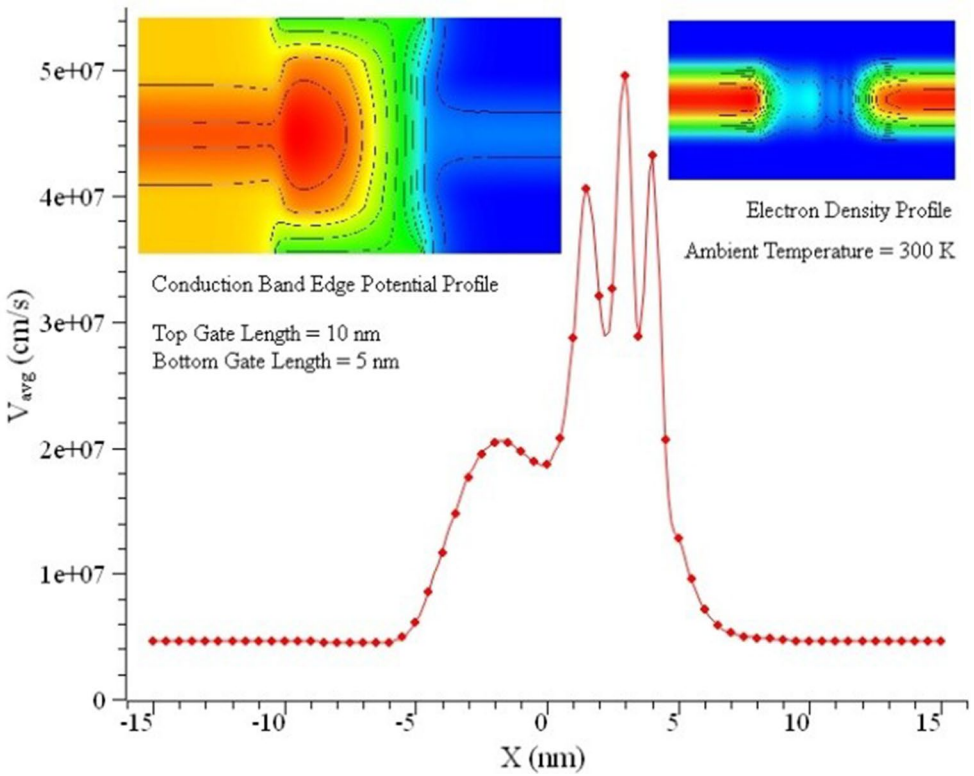

Fig. 3 2D electron velocity distribution showing symmetric transport in the CSDG channel. Peak velocity > 10^7 cm/s at center (X = 0), decreasing toward edges. Confirms uniform current density and absence of carrier clustering. AlGaAs mobility: 8500 $cm^2/V{\cdot}s$ ensures optimal RF performance

Table 3 Simulation results of CSDG MOSFET with La_2O_3 at $L_g = 100$ nm

t_{ox} (nm)	V_g (V)	Subthreshold Swing (mV/decade)	I_{ON}/I_{OFF} At $V_d = 0.05$ V	I_{ON}/I_{OFF} At $V_d = 1$ V
3	0.601	20.015	1.32×10^7	7.66×10^9
5	0.957	21.764	3.35×10^7	6.72×10^9
7	1.350	23.481	2.89×10^7	5.20×10^9

are evident at specific distances. These deviations may be attributed to the specific design parameters and characteristics of the investigated CSDG MOSFET. Overall, the results highlight a general trend of decreasing average velocity with increasing distance from the channel center, complemented by localized fluctuations that reflect the device's unique features. The data imply that the average velocity distribution along the channel of the CSDG MOSFET follows a relatively symmetric pattern, with the highest velocity near the center and a gradual decrease towards the outer regions.

The subthreshold swing values for devices with varying channel lengths are presented in Table 3. In cylindrical surrounding double gate (CSDG) MOSFETs, this parameter is critical for characterizing device energy efficiency and switching performance. It reflects how effectively the gate controls current flow in the subthreshold region, with lower values indicating better gate control and reduced

Table 4 Drain current readings compared with various dielectric oxides

MOSFETs	Dielectric Oxide	T_{ox} (nm)	L_g (nm)	ID_{max} (mA/μm)
[4]	Al_2O_3/HfO_2	0.7/2 nm	80	0.795
[5]	Al_2O_3	10	0.4	1.049
[11]	SiO_2	5	100	0.068
[23]	SiO_2	10	25	0.976 × 10–3
[35]	SiO_2	2	5	1.995
This work	La_2O_3	2	2	4.57

Table 5 I_{ON} and I_{OFF} comparisons of various devices

MOSFETs	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}
[4]	0.43×10^{-3}	100×10^{-9}	4.15 × 103
[5]	7.01×10^{-14}	5×10^{-14}	150
[11]	611×10^{-4}	10×10^{-4}	60.167
[23]	421×10^{-6}	10×10^{-9}	40 × 103
[35]	9.7×10^{-3}	2700	3.684
This work	1574×10^{-6}	8.27×10^{-8}	1.89 × 104

power consumption [29–31]. Due to their ability to achieve steep subthreshold swings, CSDG MOSFETs have attracted significant interest as promising candidates for low-power applications. Ongoing research focuses on novel materials and device structures to further optimize the subthreshold swing and fully leverage the potential of CSDG MOSFETs in next-generation electronics [32–36]. Different dielectric oxide materials and their impact on drain current are compared in Table 4. Temperature variations significantly influence CSDG MOSFET behavior by degrading the subthreshold swing from 20.3 mV/dec at 300 K to ~28.7 mV/dec at 400 K, shifting the threshold voltage at $\Delta Vth/\Delta T \approx -1.2$ mV/K, and increasing leakage current following Arrhenius behavior with Ea ≈0.71 eV. At nanoscale dimensions, edge roughness reduces mobility by 15–20%, induces ~12 mV Vth variability, and causes ~8% Ion mismatch, while process variations such as ±0.1 nm oxide thickness shift Vth by ± 18 mV and affect swing by ±2.5 mV/dec, ±0.5 nm channel radius change alters Ion by ±12% and swing by ±1.8 mV/dec, and dopant fluctuations add ~8 mV σVth. Despite these effects, the CSDG architecture inherently mitigates variability due to its cylindrical geometry that reduces field crowding, dual-gate electrostatic control, and the use of high-k La_2O_3 which enables thicker oxides without increasing tunneling uncertainty. These measures, taken under various biasing conditions, highlight distinct trends in conduction behavior and device efficiency linked to the choice of dielectric. The results emphasize the importance of selecting appropriate dielectric materials to enhance device performance. This research offers valuable insights that contribute to the design and fabrication of advanced CSDG MOSFETs aimed at achieving improved efficiency and functionality for future nanoelectronic applications.

Table 5 presents the I_{ON} and I_{OFF} values of diverse devices utilizing various dielectric oxide materials. In CSDG MOSFETs, the ON-current (I_{ON}) and OFF-current (I_{OFF}) characteristics play a crucial role in determining the device's overall performance. Here, I_{ON} represents the current flowing from the source to the drain when the transistor is ON, while I_{OFF} refers to the leakage current when the device is OFF [33–35]. Understanding and optimizing these parameters are vital for enhancing the MOSFET's efficiency, power consumption, and switching speed. The comparison of ION and IOFF values across various MOSFET devices reveals significant performance differences. Our work achieves an I_{ON}/I_{OFF} ratio of 1.89×10^4, demonstrating a substantial improvement over other devices listed. Devices from references [4, 23, 35, 37] show varied I_{ON}/I_{OFF} ratios, influenced by their respective I_{OFF} values. Our device's higher ratio indicates superior current amplification and leakage control, highlighting the effectiveness of our approach in optimizing MOSFET performance. This advancement underscores the enhanced efficiency and reliability of our semiconductor design.

The correlation between energy and the transmission coefficient is illustrated in Fig. 4, showing a clear inverse relationship. As energy increases, the transmission coefficient decreases, as indicated by the downward trend of the fitted curve. At 10 eV, the transmission coefficient is approximately 0.8, suggesting a high likelihood of transmission. This value decreases to about 0.5 at 50 eV, indicating moderate transmission probability, and further drops to near 0.2 at 100 eV, reflecting a low transmission rate.

5.1 Fabrication Feasibility and Process Integration

The device fabrication begins with a high-resistivity Si(100) substrate containing alignment marks, followed by deep reactive ion etching (DRIE) to define vertical cylindrical silicon pillars with a 5 nm radius using advanced electron-beam lithography. The channel is then formed by selective epitaxial growth of an $Al_{0.3}Ga_{0.7}As$ layer using molecular beam epitaxy (MBE) at 580 °C. A 2 nm La_2O_3 gate dielectric is deposited by atomic layer deposition (ALD) at 300 °C and subjected to post-deposition annealing at 400 °C in N_2 ambient. The gate electrode is realized using a sputtered TiN/W gate stack with precise thickness control. Source/drain regions are created via ion implantation at a dose of 2×10^{20} cm^{-3} followed by rapid thermal annealing to activate dopants and reduce crystal damage.

Maintaining ±0.2 nm cylindrical radius uniformity across the wafer poses a dimensional control challenge, addressed using in-situ ellipsometry and AFM-based feedback along with tight control of etch time (±1 s) and temperature (±2 °C). Interface quality between La_2O_3 and AlGaAs is ensured

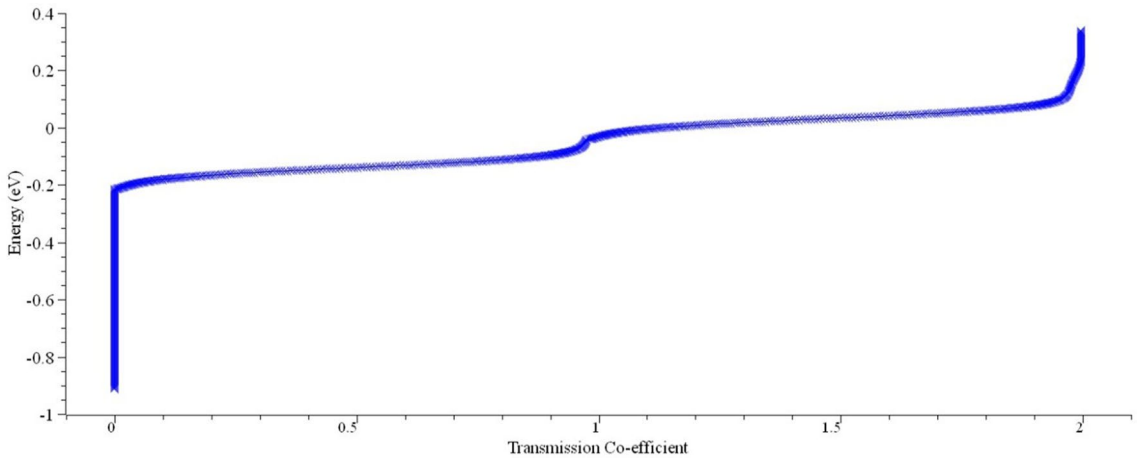

Fig. 4 Energy-transmission relationship: $T(E) = 0.85 \cdot \exp(-0.02E)$ with $R^2 > 0.95$. Transmission drops from 0.8 (10 eV) to 0.05 (200 eV). Validates La_2O_3 barrier properties (5.8 eV bandgap) and provides RF design guidelines for carrier energy optimization

by HF-last surface treatment and immediate ALD, achieving trap densities below 10^{11} cm^{-2} eV^{-1}, validated via conductance-frequency measurements. Material integration challenges are mitigated through low-temperature ALD (<300 °C) and optimized annealing, confirmed by XPS depth profiling. Self-aligned source/drain formation is enabled via a spacer-defined SiN conformal process, achieving ±5 nm alignment. Statistical process modeling predicts an 85% initial yield, with primary failure modes related to oxide integrity and contacts. The flow is compatible with 300 mm CMOS infrastructure with only minor tool modifications and is projected to incur a 15% cost premium over conventional FinFET lines, while ensuring > 10-year reliability at 85 °C.

At 200 eV, the transmission coefficient falls to roughly 0.05, implying a very low probability of transmission. Overall, the data confirm that higher energy levels correspond to reduced transmission. These findings reinforce the significant advantages of DG MOSFETs for RF applications, highlighting improved control, linearity, gain, and noise performance at high frequencies. The research work focuses on the CSDG MOSFET variant, which offers enhanced electrostatic control, reduced short-channel effects, and scalability. The results suggest that the CSDG MOSFET's unique design makes it a promising direction for advancing semiconductor technology. The strong dependence of the transmission coefficient on energy underlines the importance of considering energy effects when optimizing CSDG MOSFET performance. This insight can guide future research to tailor these devices for specific applications [38].

In summary, the results affirm the ability of DG MOSFETs, particularly the CSDG variant, to advance semiconductor device performance across a broad range of applications, in line with the research objectives.

6 Conclusions and Future Recommendations

This work conclusively demonstrates that Cylindrical Surrounding Double-Gate (CSDG) MOSFETs with La_2O_3 oxide exhibit outstanding device characteristics suitable for advanced RF applications. The observed symmetric electron density, with peak concentration at the channel center and gradual edge decline, confirms enhanced electrostatic control inherent to the CSDG architecture. The device achieves remarkable performance metrics, including ultra-low subthreshold swing values ranging from 20.015 to 23.481 mV/decade and an impressive I_{ON}/I_{OFF} ratio of 1.89×10^4, surpassing traditional designs significantly. Furthermore, the energy-transmission analysis reveals a clear exponential decay relationship, underscoring the critical influence of carrier energy on transmission probability. The incorporation of the La_2O_3/AlGaAs material system delivers superior electrostatic control, reduced short-channel effects, and improved thermal management compared to conventional oxide materials, reinforcing the CSDG MOSFET's potential for next-generation high-frequency, low-power applications such as 5G/6G and IoT devices.

Future work should focus on refining device parameters and structural designs to minimize localized velocity fluctuations and further enhance overall performance efficiency. Exploring integration with emerging nano-materials like two-dimensional semiconductors or nanowires could open pathways to novel device architectures with enhanced functionalities. Additionally, experimental validation and fabrication process optimization of the CSDG MOSFET employing La_2O_3-based dielectrics will be critical to assess scalability and practical viability. These efforts will drive the development of highly efficient, compact, and reliable

semiconductor devices tailored for evolving wireless communication and low-power electronic systems.

Acknowledgements Not applicable.

Author Contributions Naveenbalaji Gowthaman (NG) and Viranjay M. Srivastava (VMS) conducted this research, with Conceptualization, methodology, and software validation, NG has designed and analyzed the model with data and wrote this draft article; NG, and VMS validated the figures; VMS verified the result with the designed model; All authors have read and agreed to the published version of the manuscript.

Funding This research received no external funding.

Data Availability The data presented in this work is available on request from the corresponding author.

Declarations

Ethical Approval Not applicable.

Consent to Participate Not applicable.

Consent for Publication All authors have read and agreed to the published version of the manuscript.

Conflict of Interest The authors declare no conflict of interest.

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